Status of the SIR program for TELIS

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Status of the SIR program for TELIS

Outline

- TELIS requirements for SIR channel. Concepts of PL SIR for TELIS
- Design of SIR for TELIS
- FFO for TELIS, PL operation
- Optimization of HM design and regimes
- Computer control of SIR operation
- First test results of T2 SIR
- Conclusion

Main parameters of TELIS-SIR spectrometer

##	Description	Base line	Goal
1	Input frequency range, GHz	600 - 650	500-650
2	Minimum noise temperature in the range (DSB), K	200	250
3	Output IF range, GHz	5 - 7	4 - 8
4	Spectral resolution, MHz	1	1
5	Contribution to the nearest spectral channel by phased locked FFO (dynamic range), dB	-20	-20
6	Contribution to a spectral channel by phased locked FFO at 4-8 GHz offset from the carrier, K	20	20
7	LO frequency net (distance between nearest settings of the PL FFO frequency), MHz	< 300	< 300
8	Dissipated power at 4.2 K stage (including IF amplifiers chain), mW	100	50
9	Operation temperature, K	< 4.5	< 4.5

Requirements for TELIS-SIR spectrometer

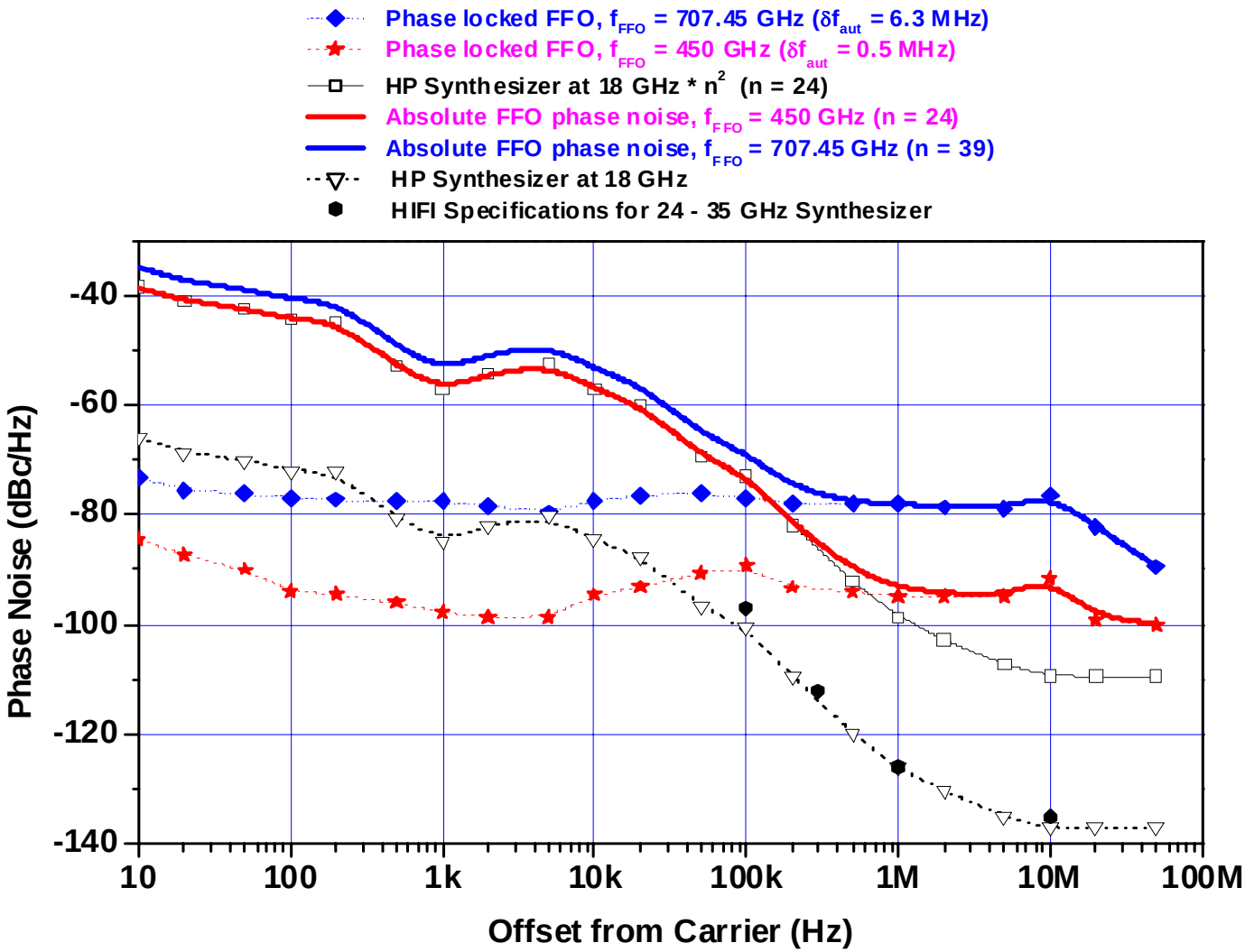
- **## 5 – required dynamic range of the spectrometer - 20 dB. It corresponds to PL FFO Phase Noise –80 dBc/Hz at the 1 MHz offset from the carrier)**
- **What about remote channels (10 –100 MHz offset) ? Do we need "1/f reduction" as required for WBS-HIFI ? That corresponds to -100 dBc/Hz at 10 MHz offset !!**

- **## 6 Contribution to a spectral channel by phased locked FFO at 4-8 GHz offset from the carrier should be < 10% of SIR Tr (< 20 K). It corresponds to :**

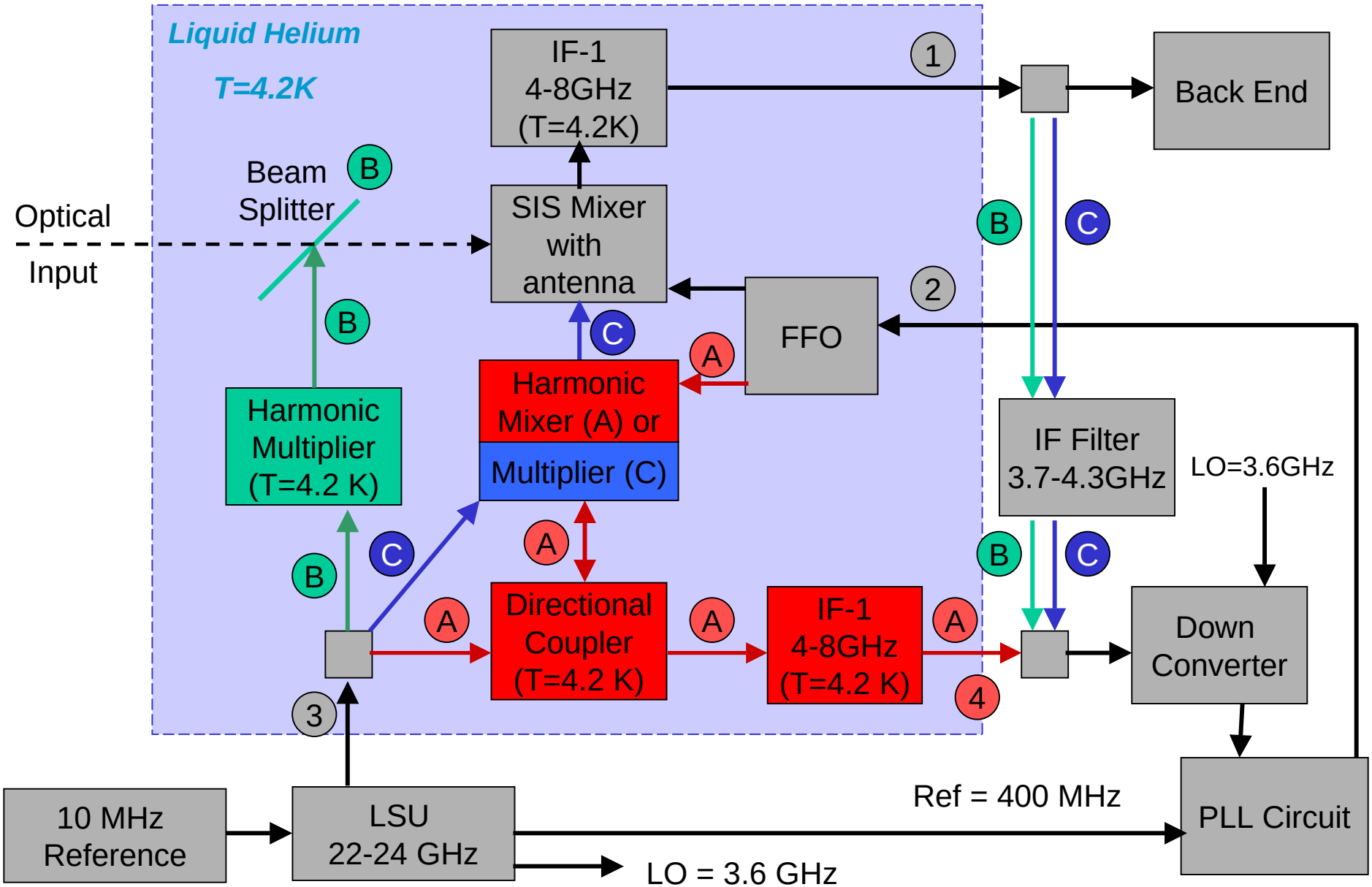
  NCR = 10 log (T_{LO}* k_B) – 10 log (P_{LO}^{opt}) = -152 dBc/Hz

- **An additional argument for balanced integrated receiver !**

Phase Noise of the PL FFO



3 Concepts of a SIR with PL FFO

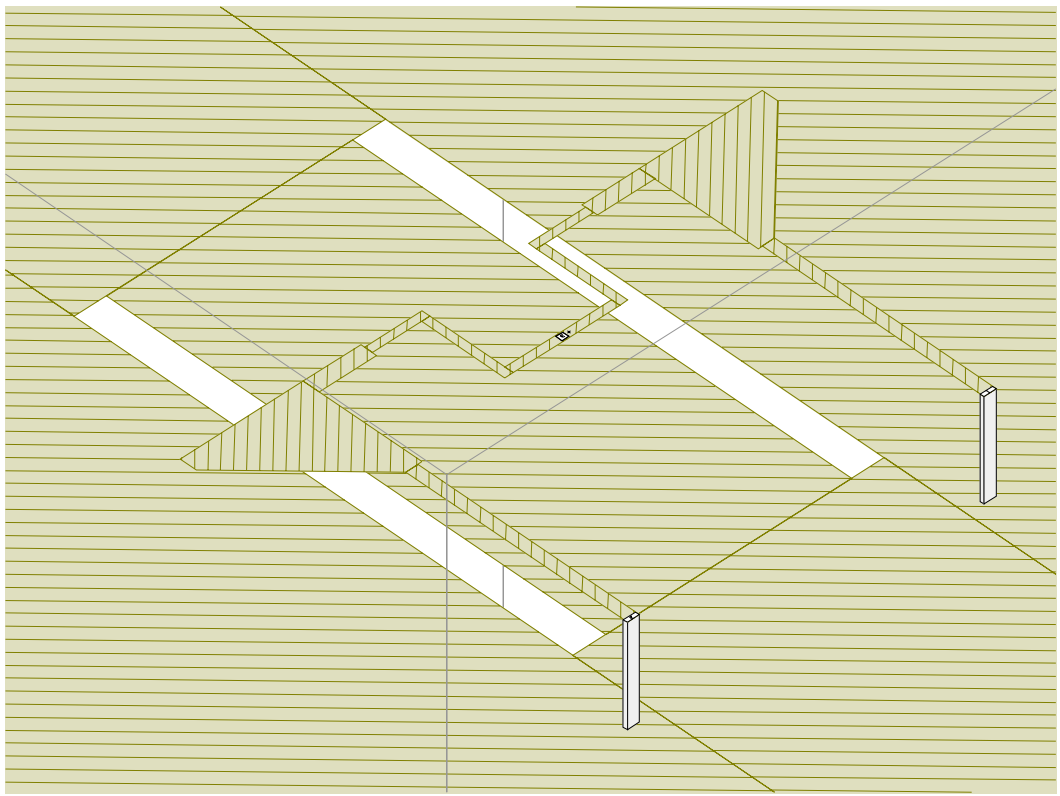


Challenges in SIR Design: Requirements

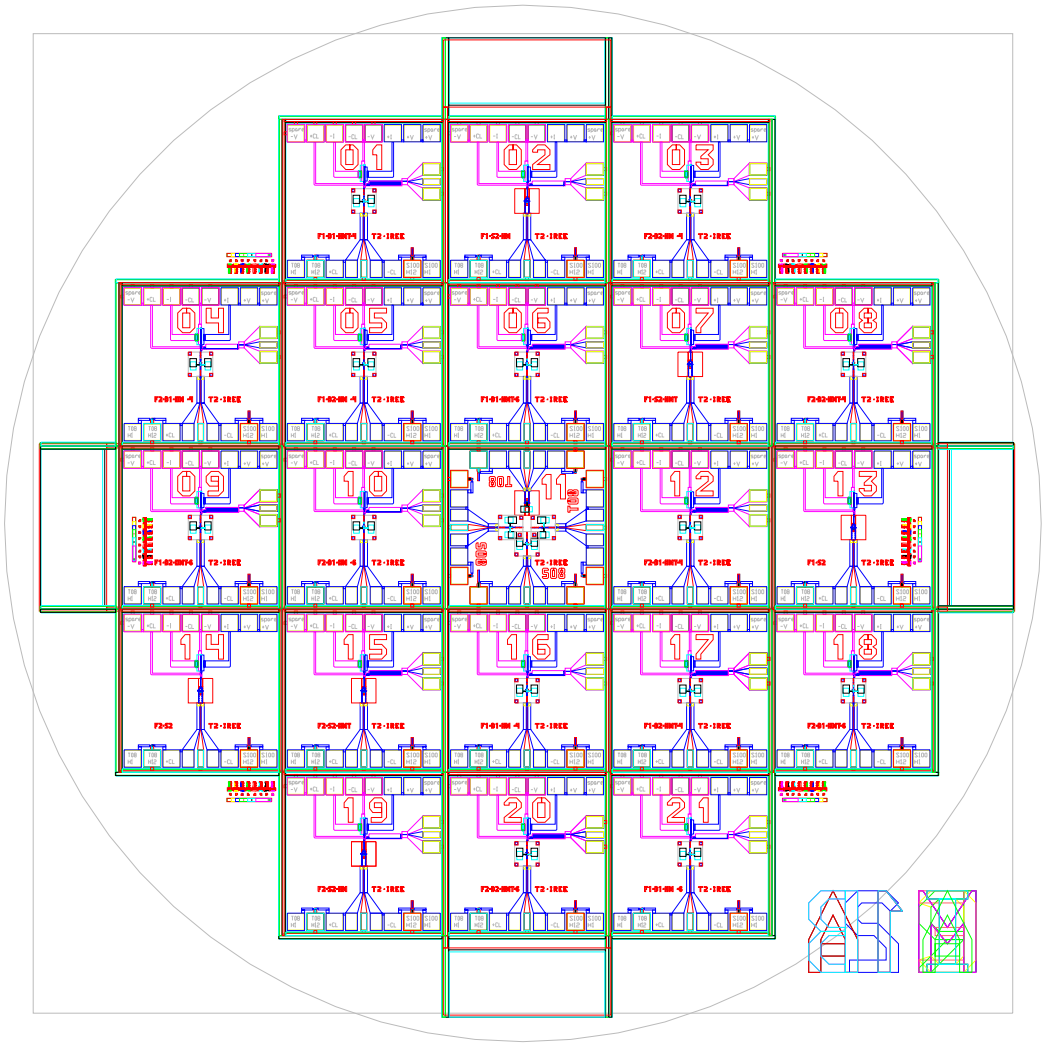
- ***500-650 GHz SIS mixer***
  - SSB Trx < 250 K @ 600-650 GHz
  - ➢ Twin-SIS is the most suitable solution
- ***Wide-band IF (4-8 GHz) coupling circuit***
  - High capacitance of the structure
- ***LO match & Integration of PLL circuit***
  - FFO operates above the boundary voltage
  - Exact power split at the antenna-mixer
  - Minimum power for HM
  - ➢ External harmonic generator as a safe option

Design Novelties: 3-D EM Modeling

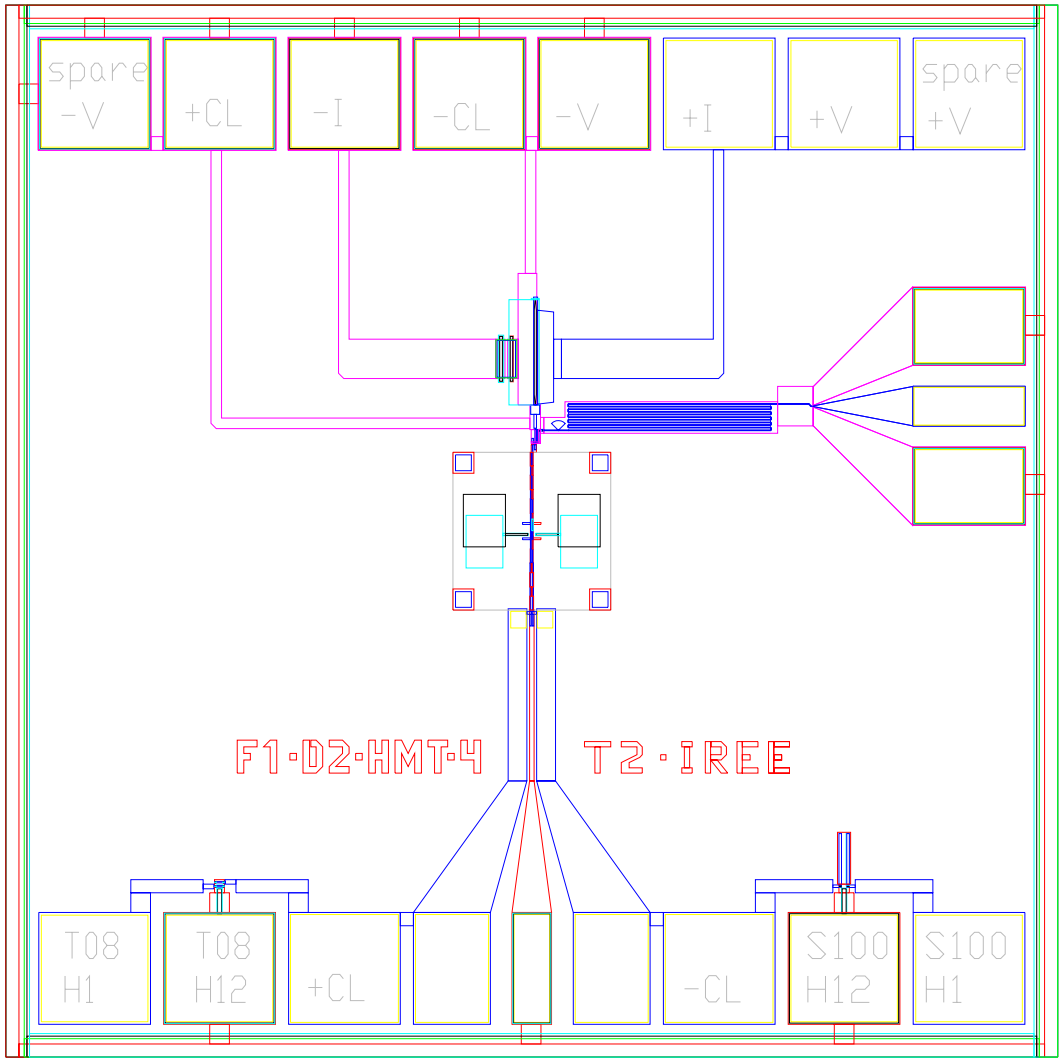
Double-Slot Antenna (DSA) Mixer



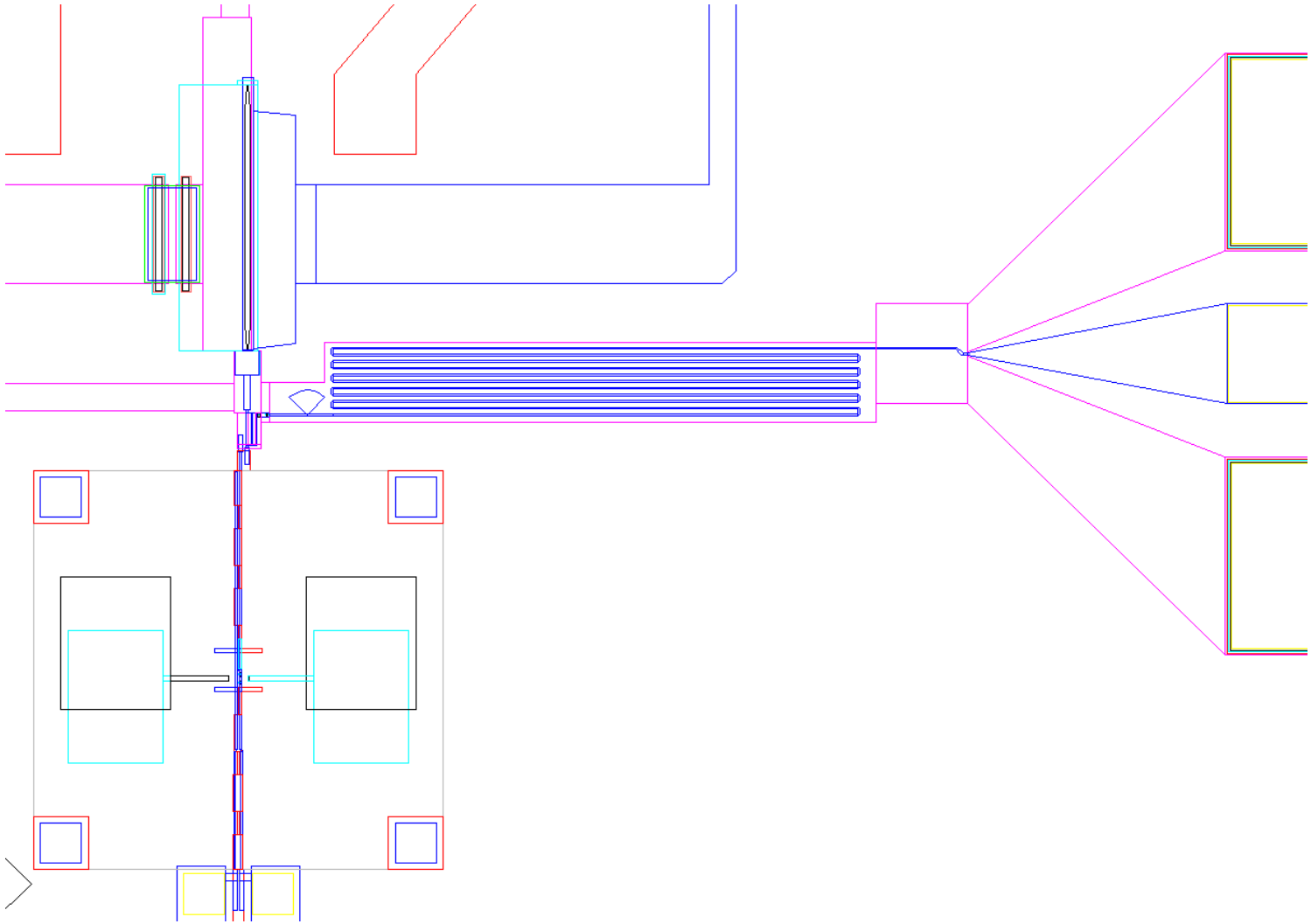
Mask Set T2:Wafer Layout



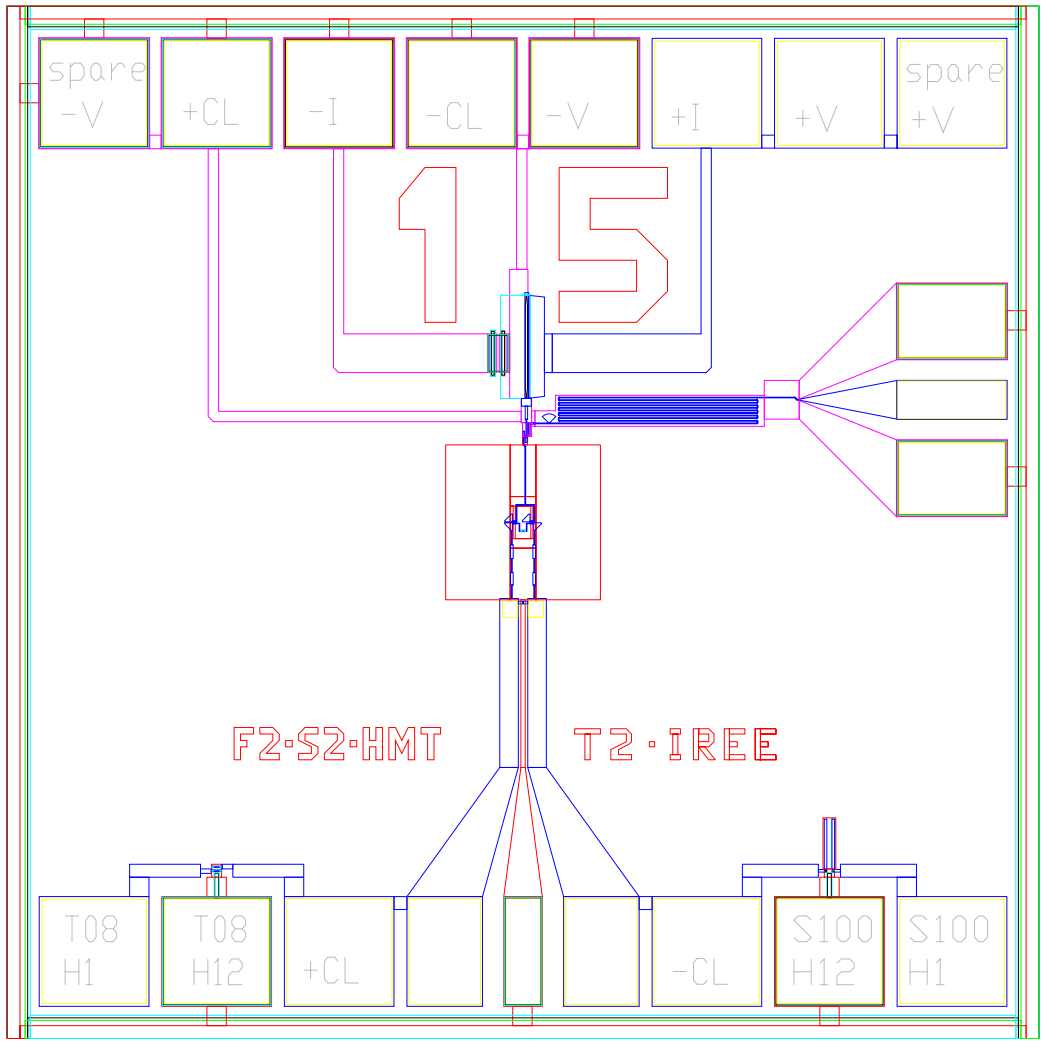
Mask Set T2: SIR DDA Chip Layout



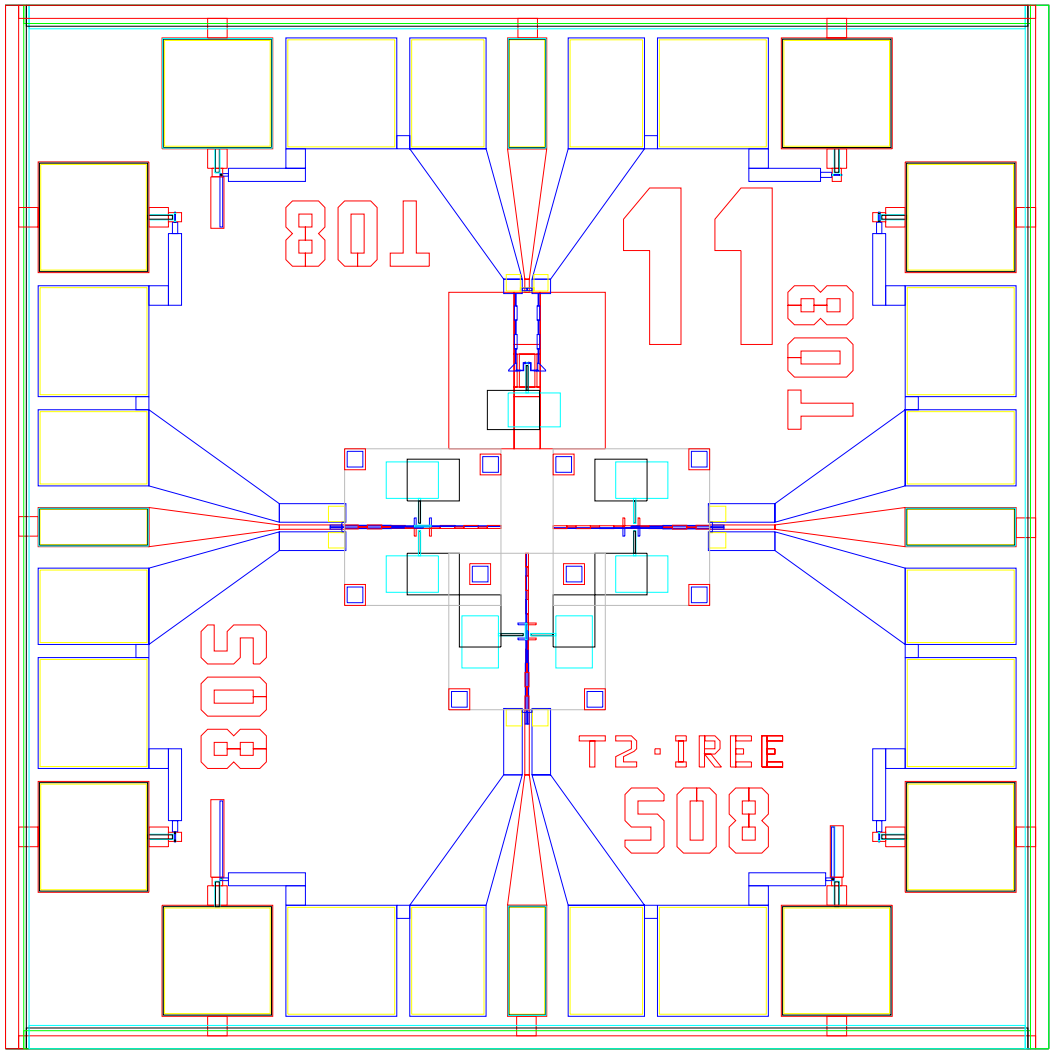
Mask Set T2: DDA Layout (magnified)



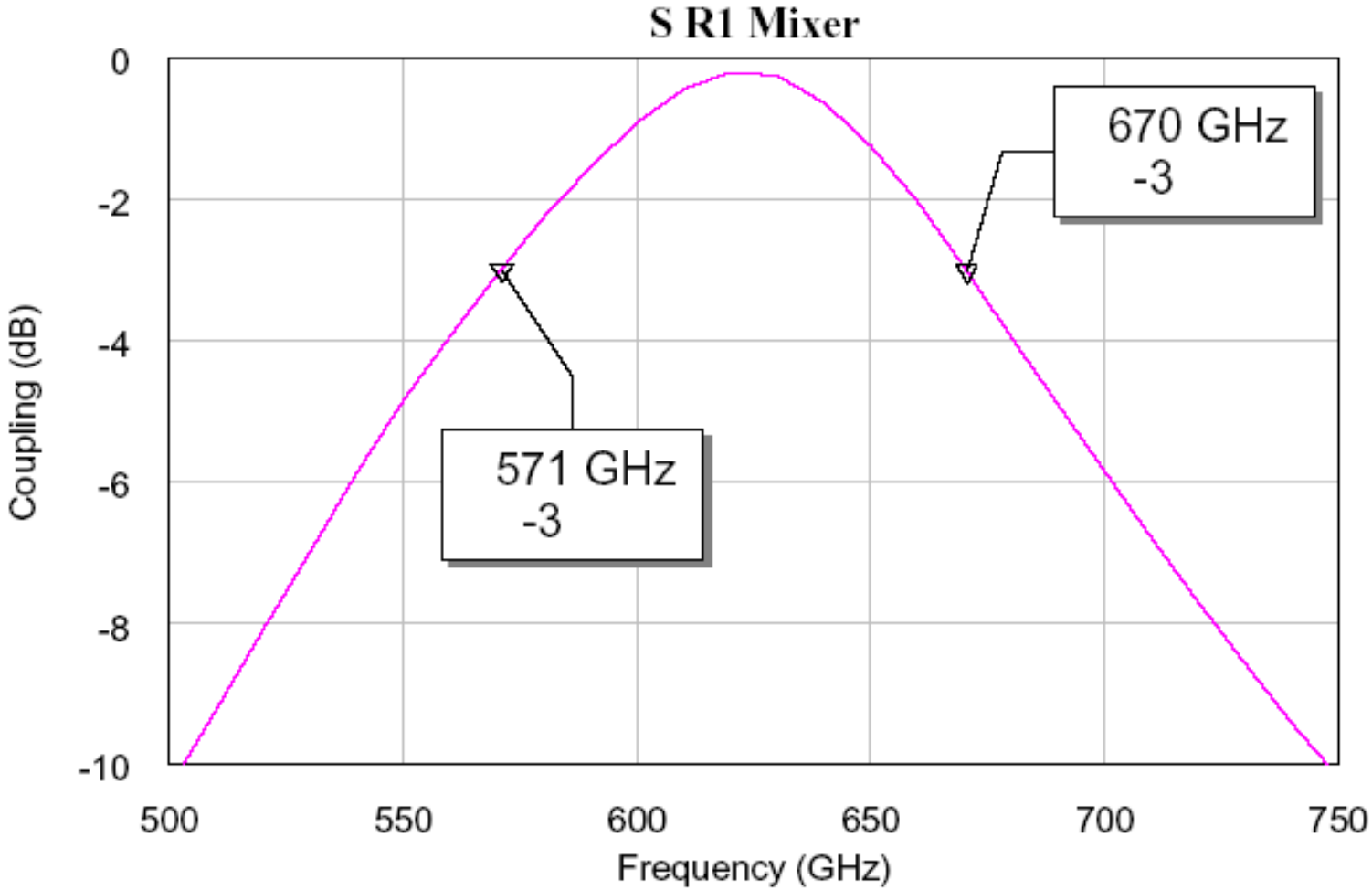
Mask Set T2: SIR DSA Chip Layout



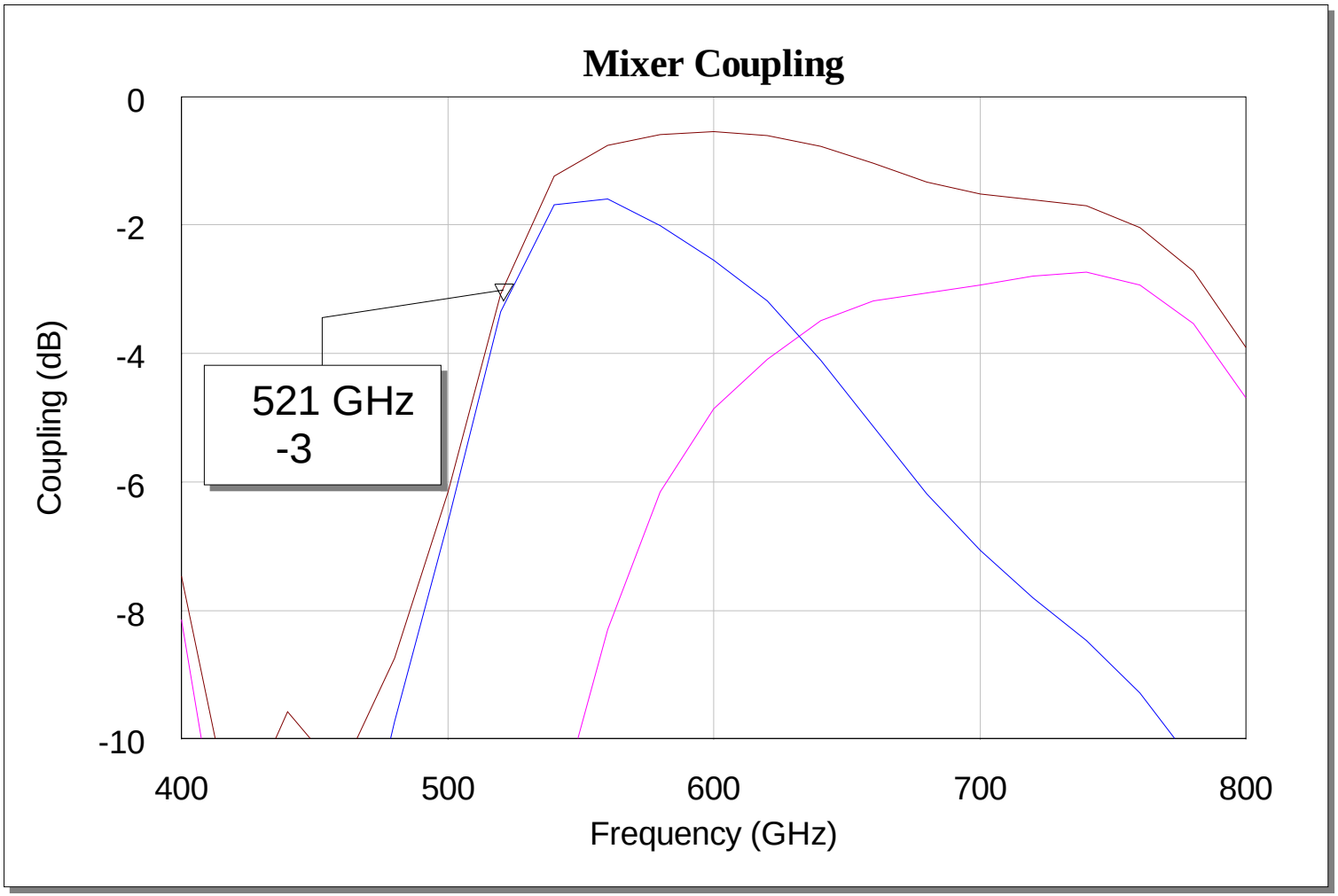
Mask Set T2: Reference Chip Layout



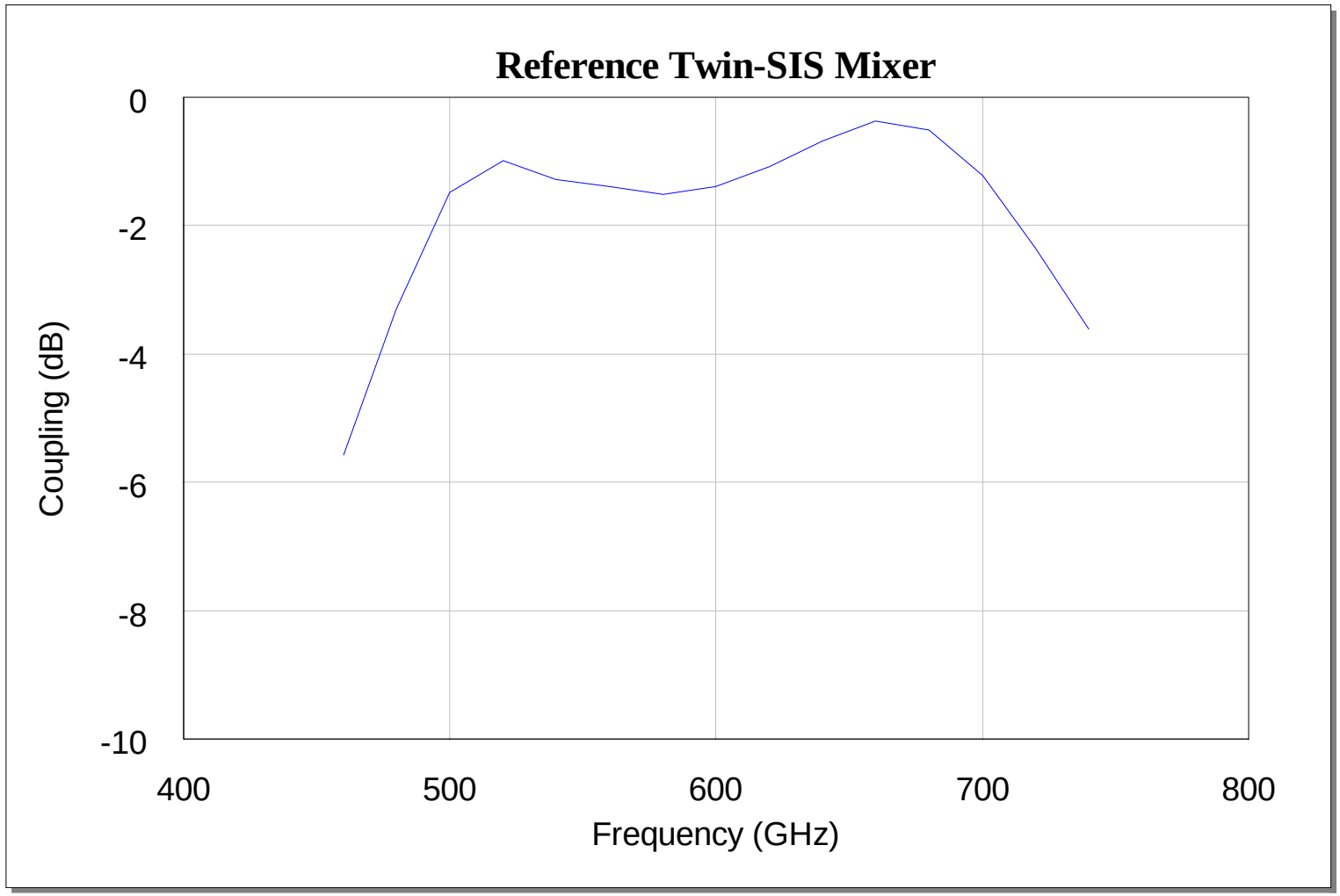
Numerical Simulations: Single-SIS DDA Mixer



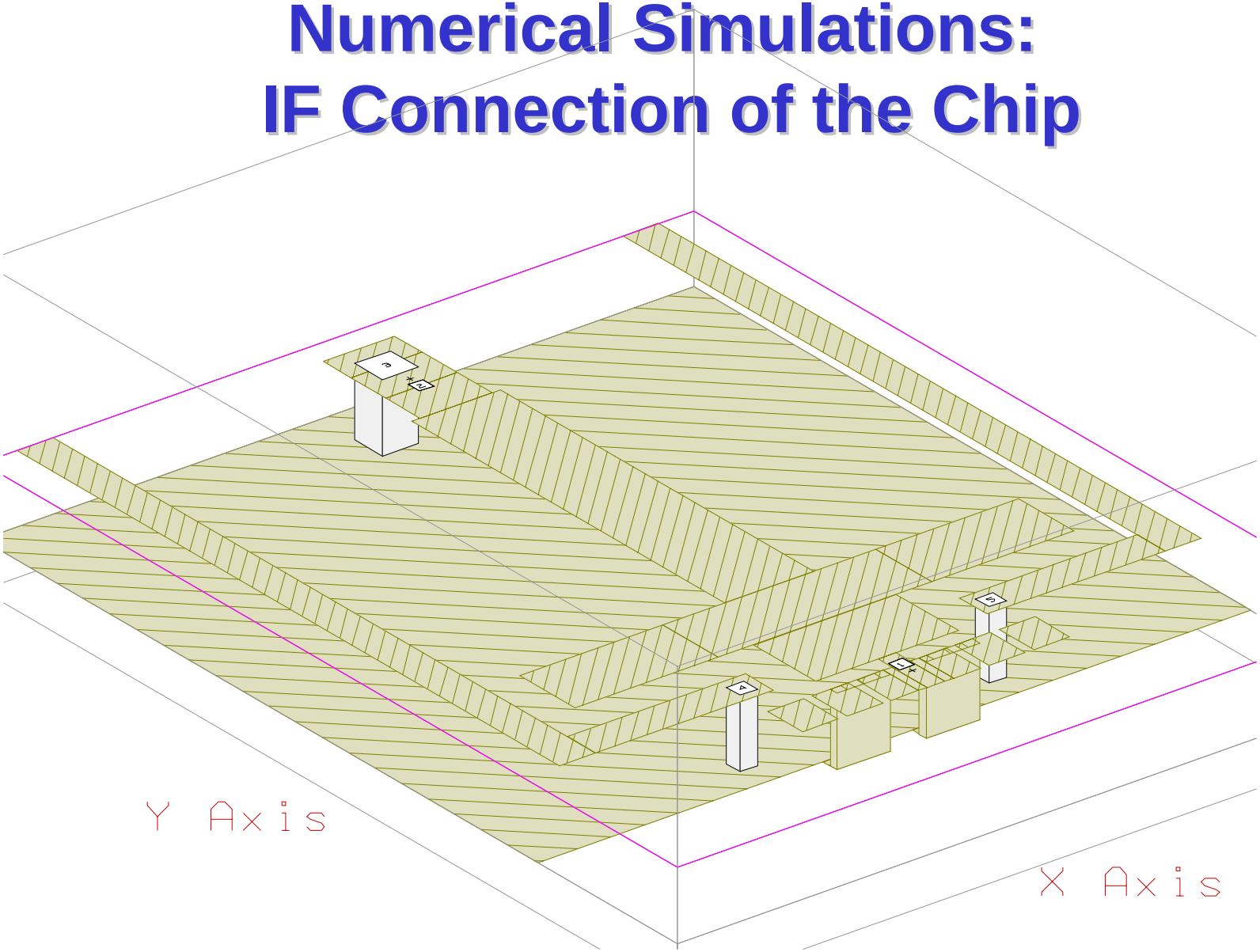
Numerical Simulations: Twin-SIS DDA Mixer



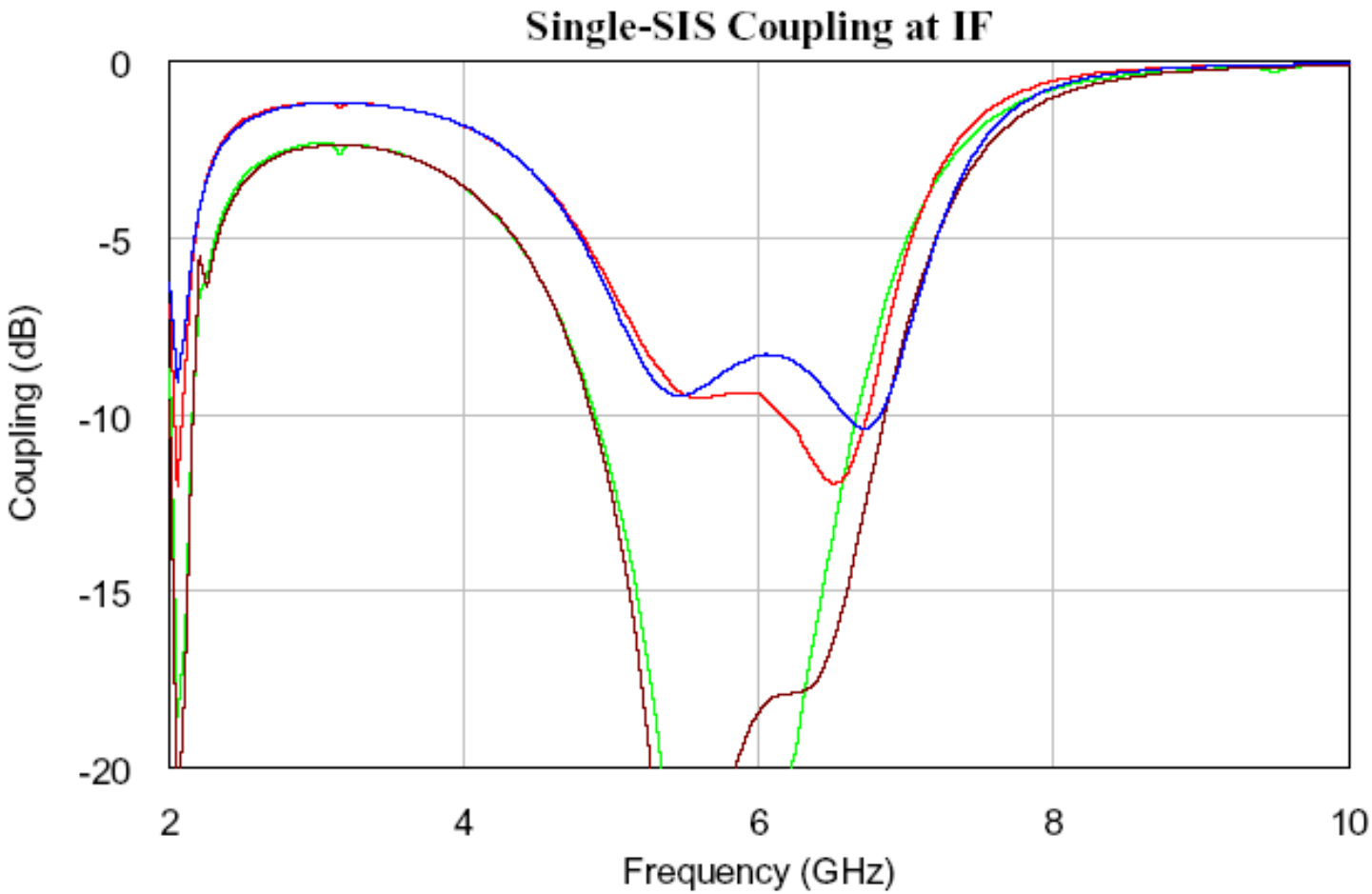
Numerical Simulations: Twin-SIS DSA Mixer



Numerical Simulations: IF Connection of the Chip



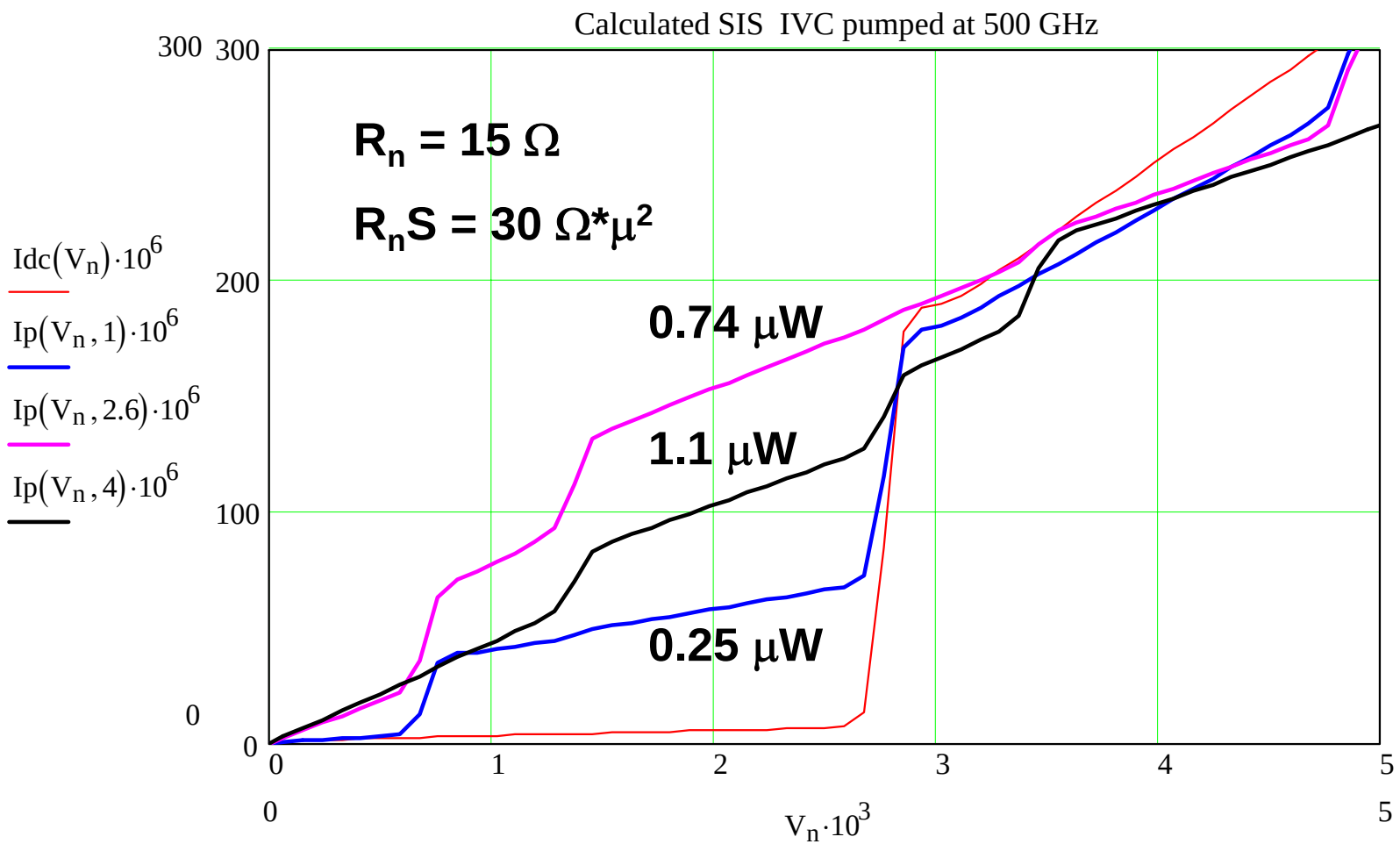
Numerical Simulations: IF Connection of the Chip



FFO for TELIS (Outline)

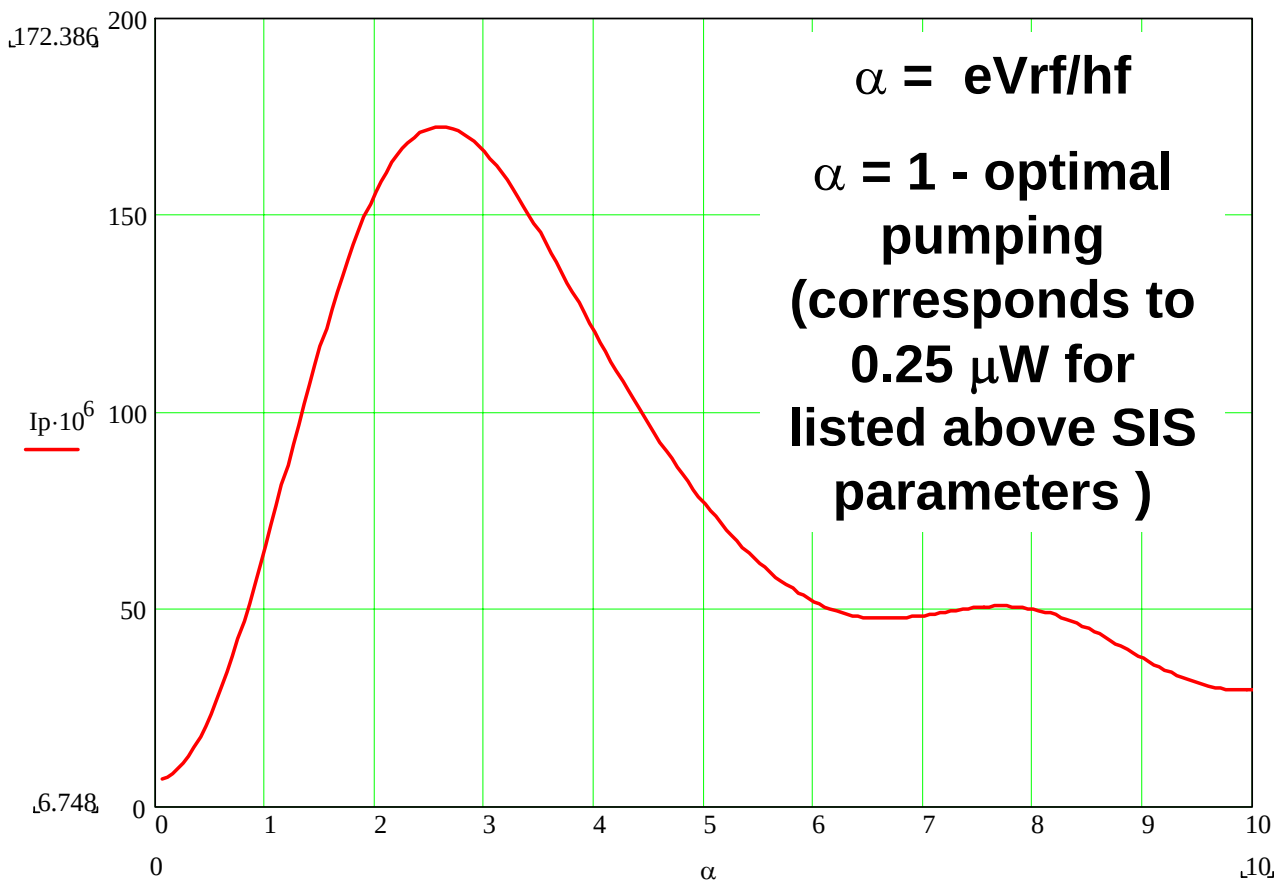
- FFO power (dependence on design)
- FFO linewidth (dependence on design, FFO frequency and current density)
- ➔ FFO for T-2
- PLL results
- FFO IVCs reproducibility, other issues
- Conclusion

Calculated IVCs of SIS mixer at different levels of power, delivered to mixer at 500 GHz

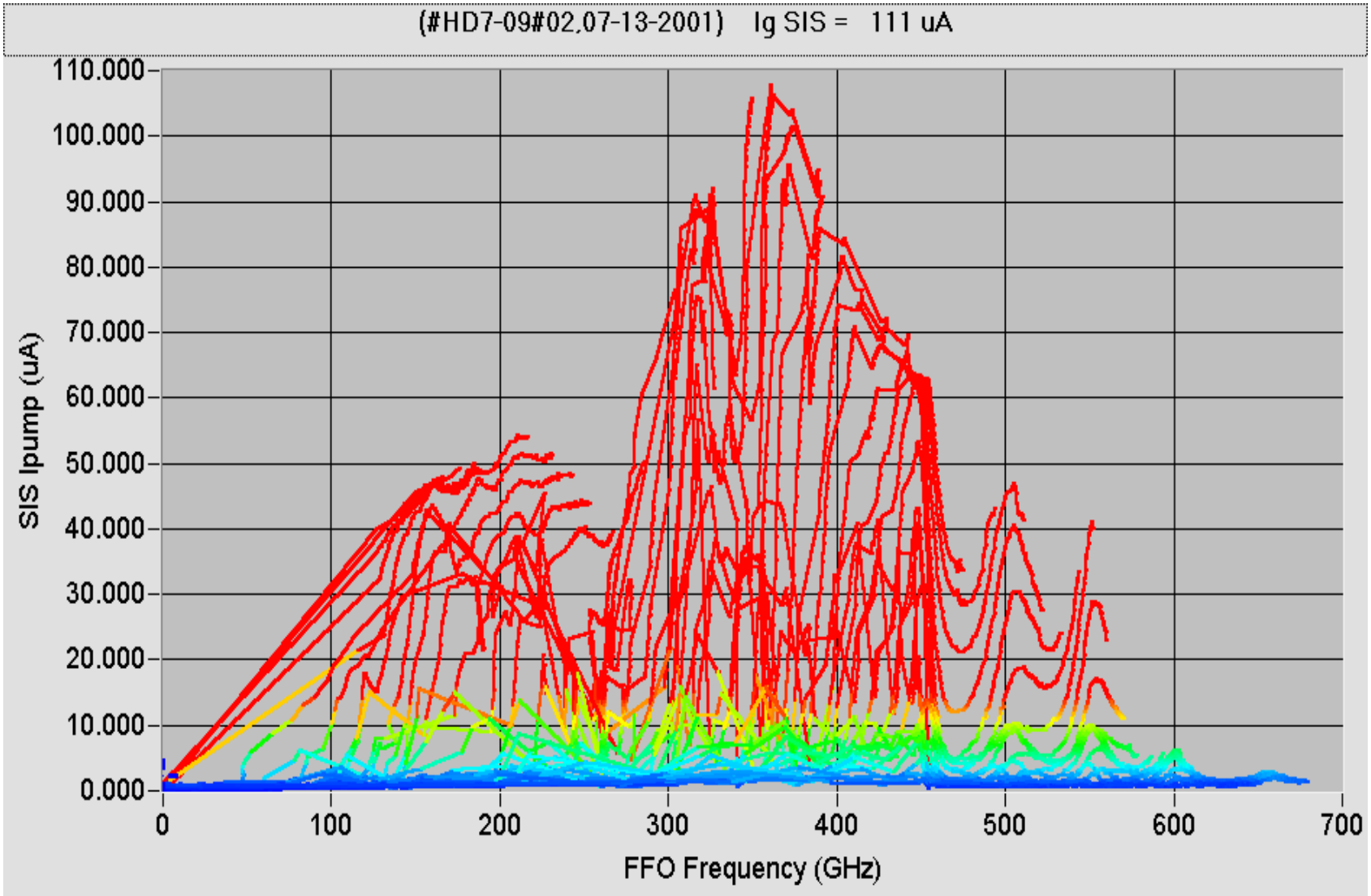


Dependence of the current on photon induced step on power

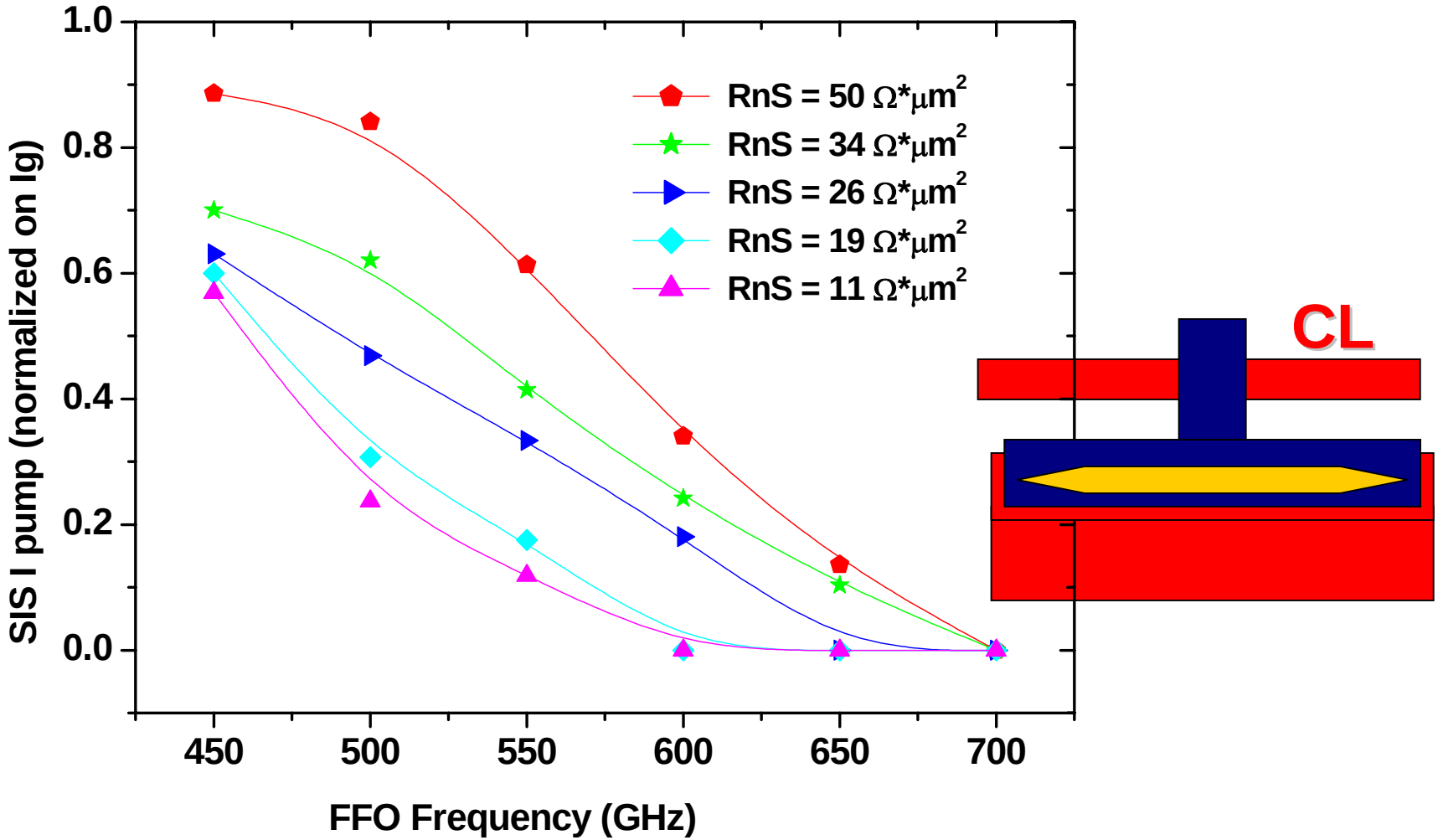
R_n = 15 Ω; R_nS = 30 Ω*μ²; f = 500 GHz; Vsis = 2.5 mV



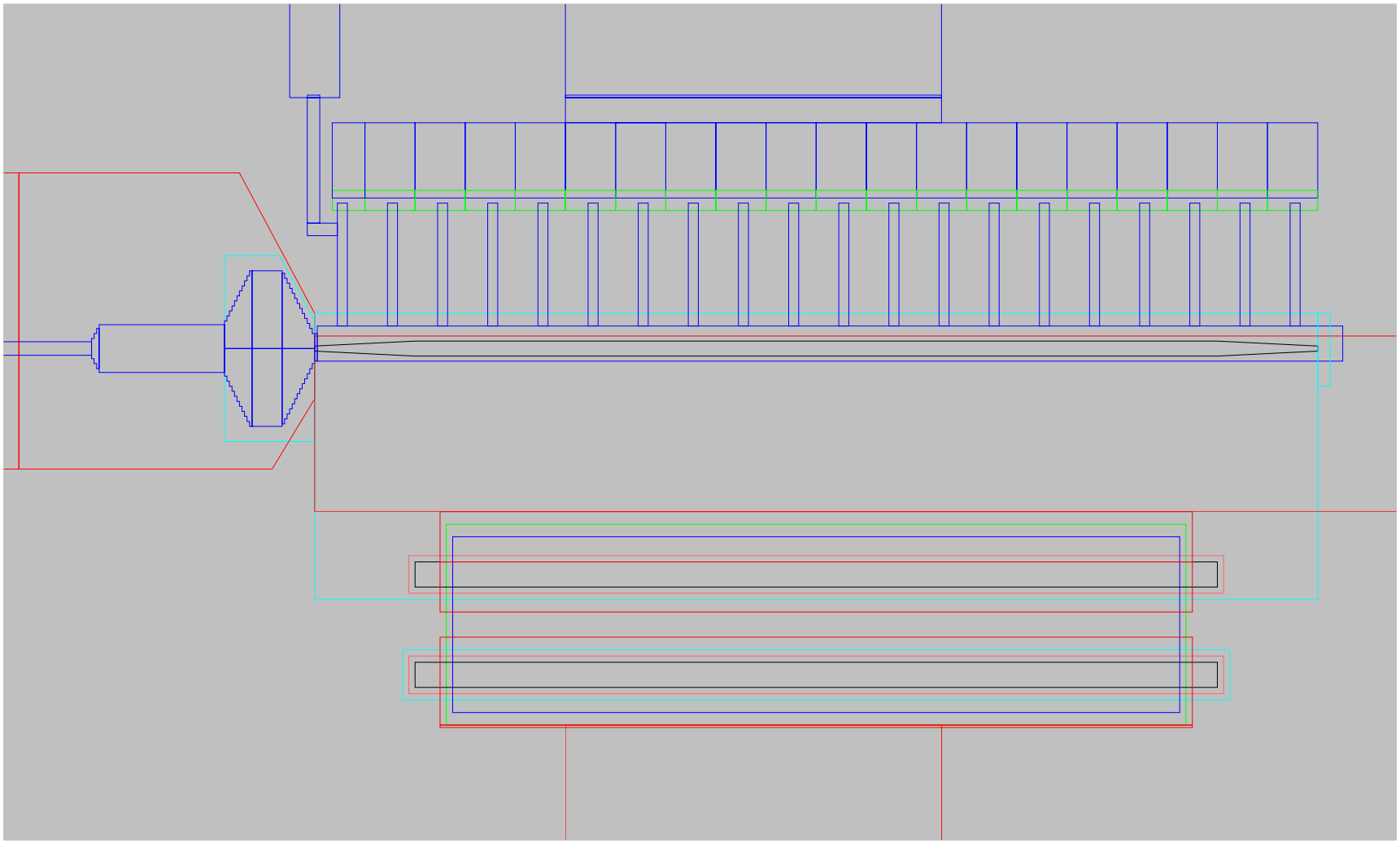
HD7-09#02 (RnS = 26 Ω*μ²)



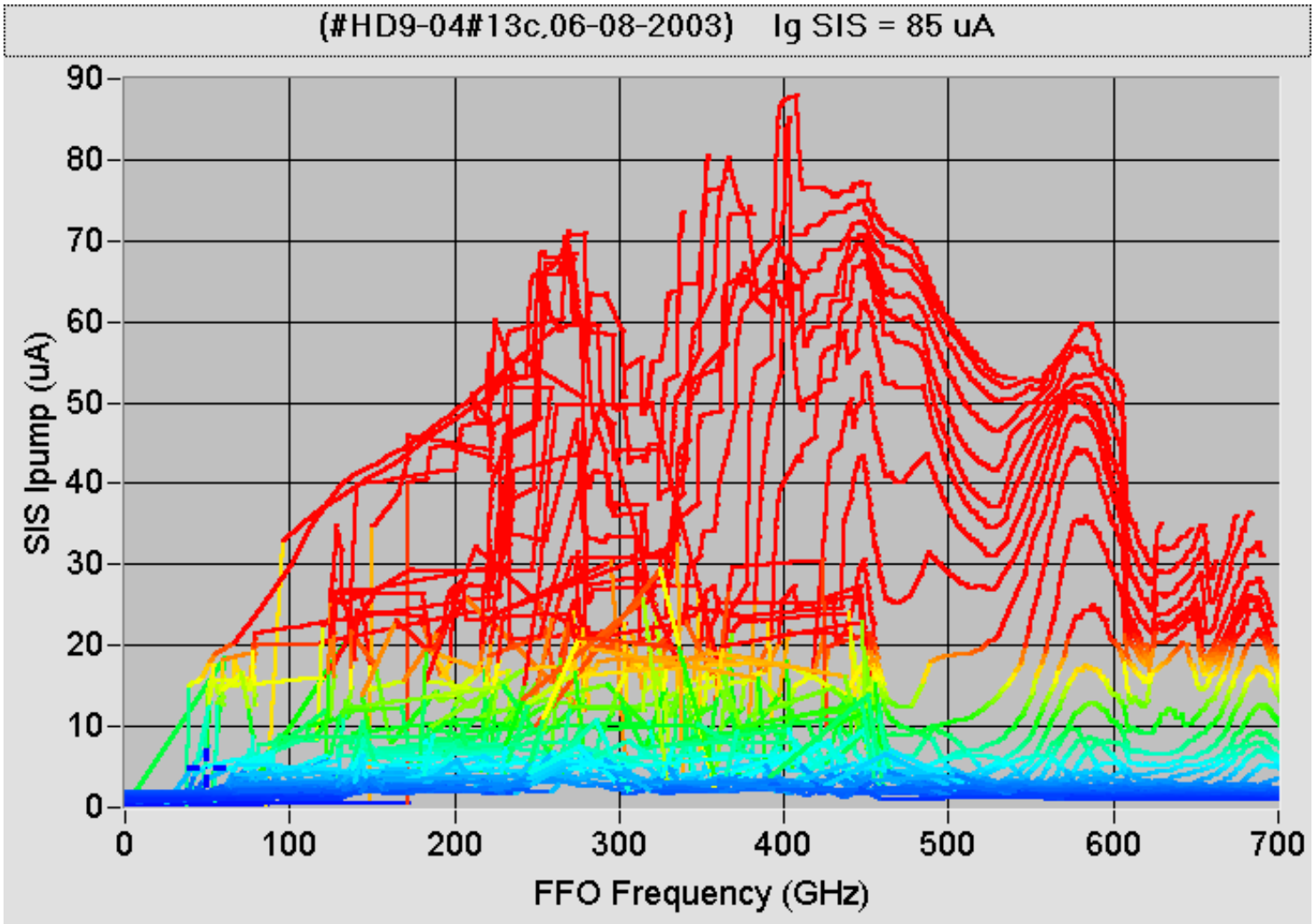
SIS Pumping by FFO (HD7 & T1 design)



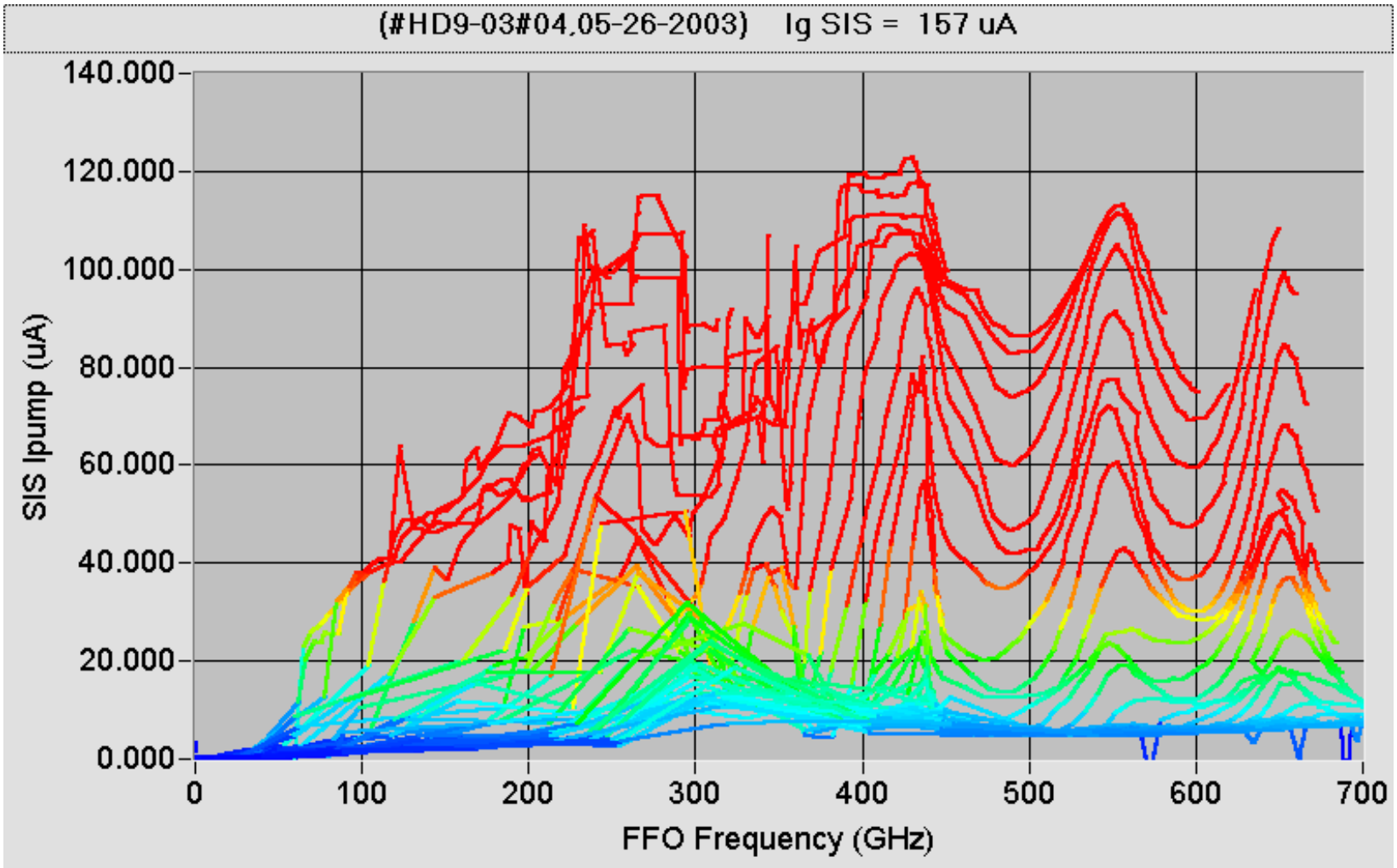
New FFO design HD9 with distributed bias



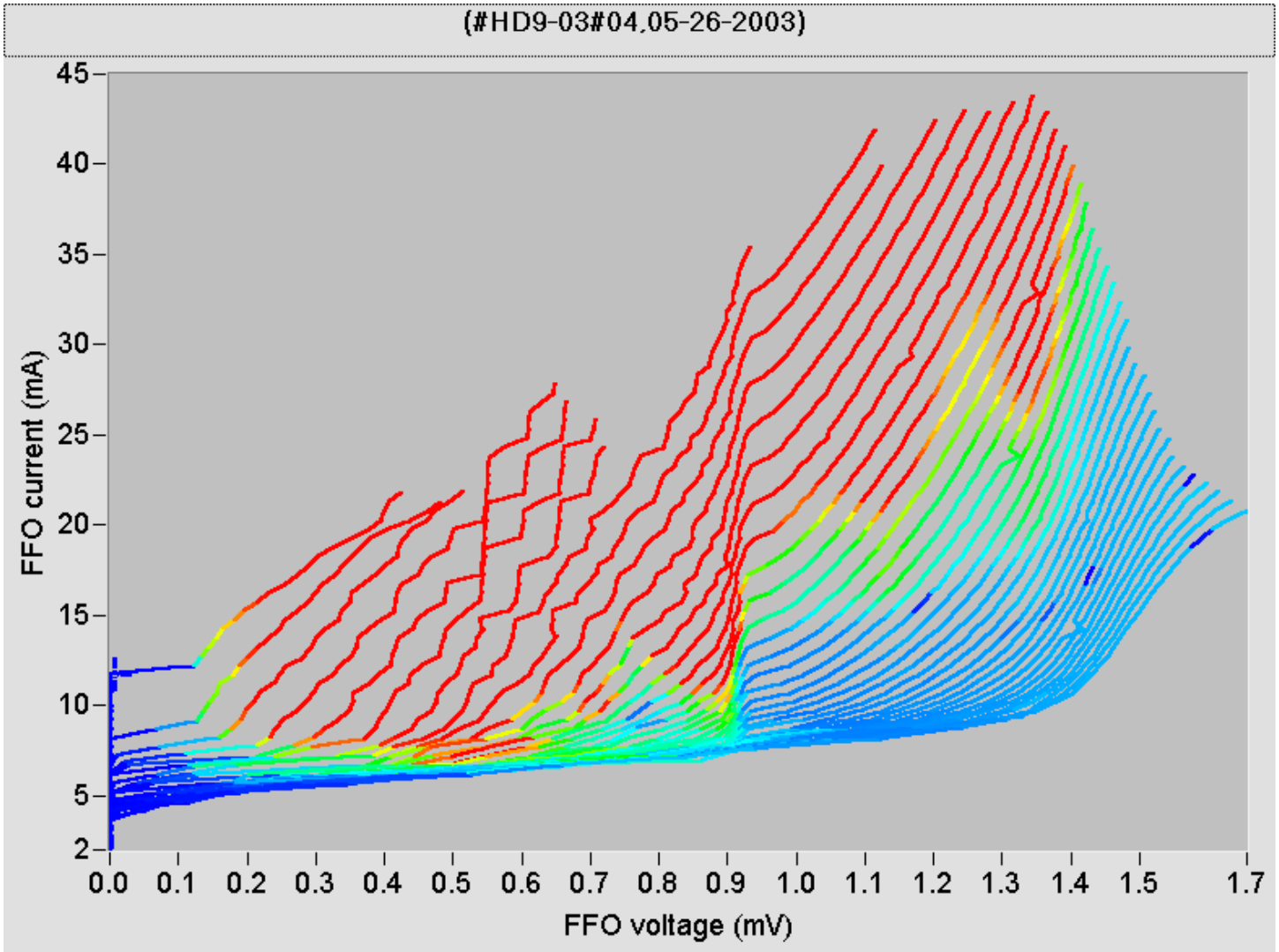
HD9-04#13 (RnS = 37 Ω*μ²)



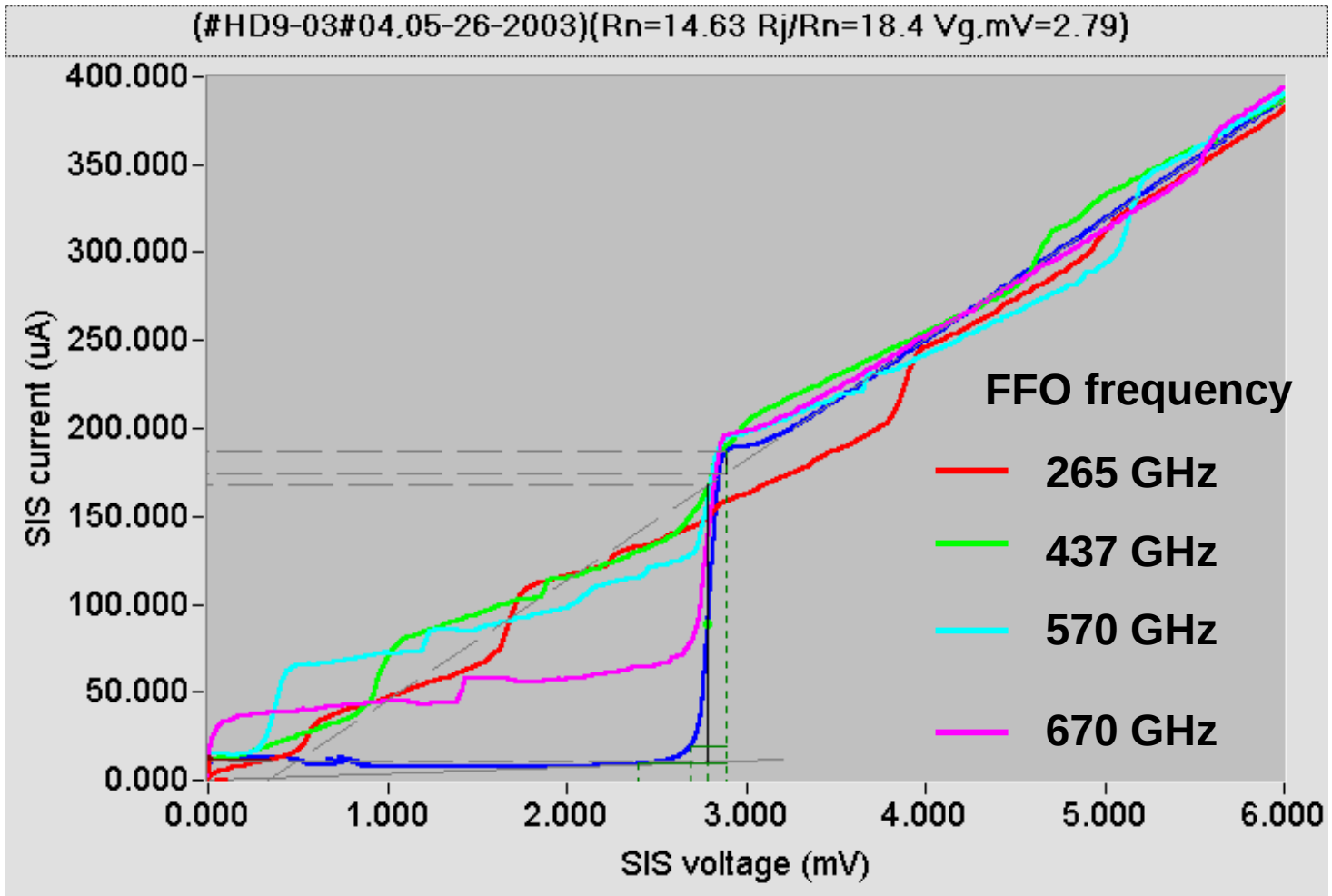
HD9-03-04 (RnS = 27.5 Ω*μ²)



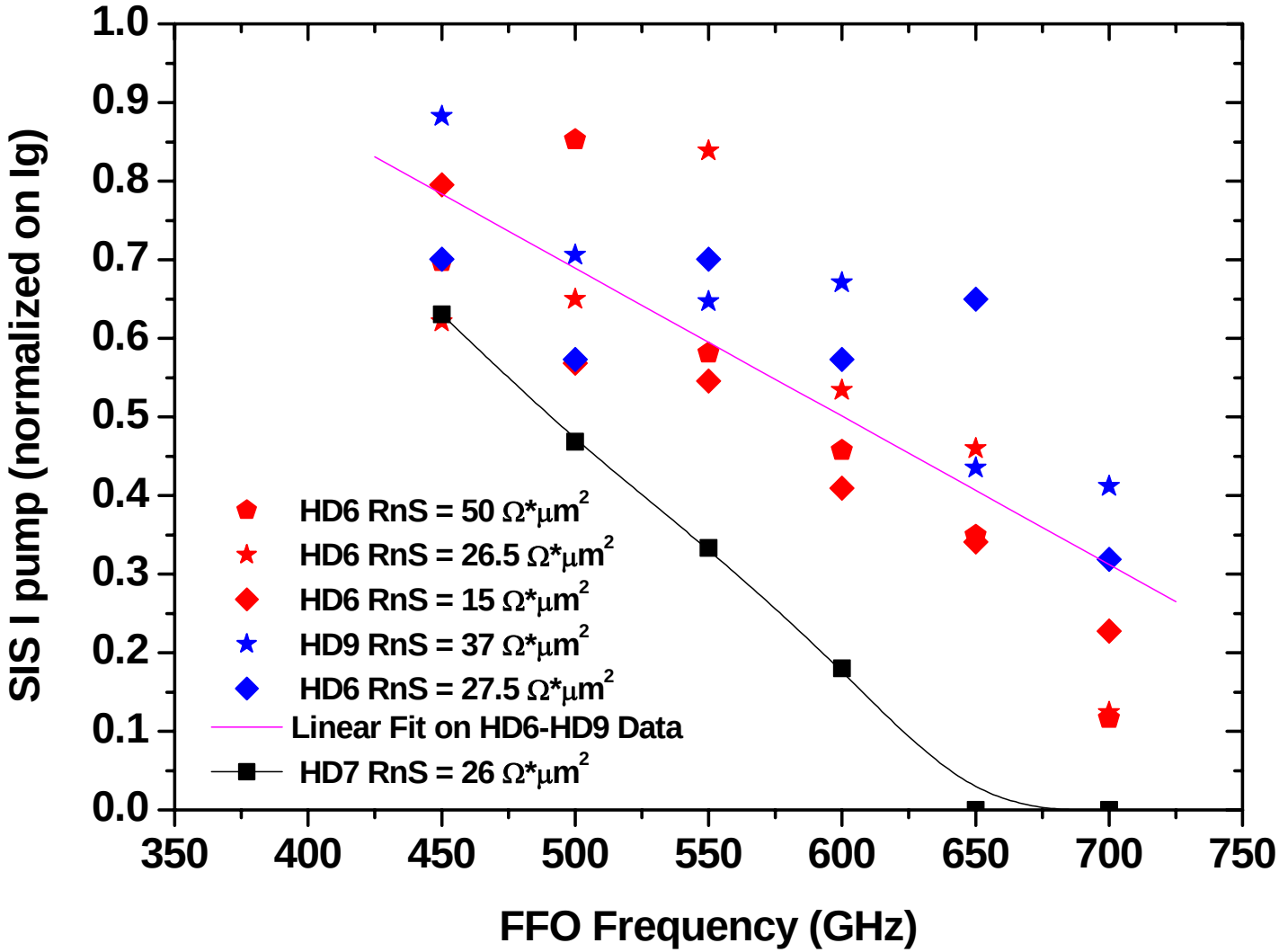
FFO IVCs - HD9-03-04 (RnS = 27.5 Ω*μ²)



HD9-03#04; SIS pumped by FFO RnS = 27.5 Ω*μ²



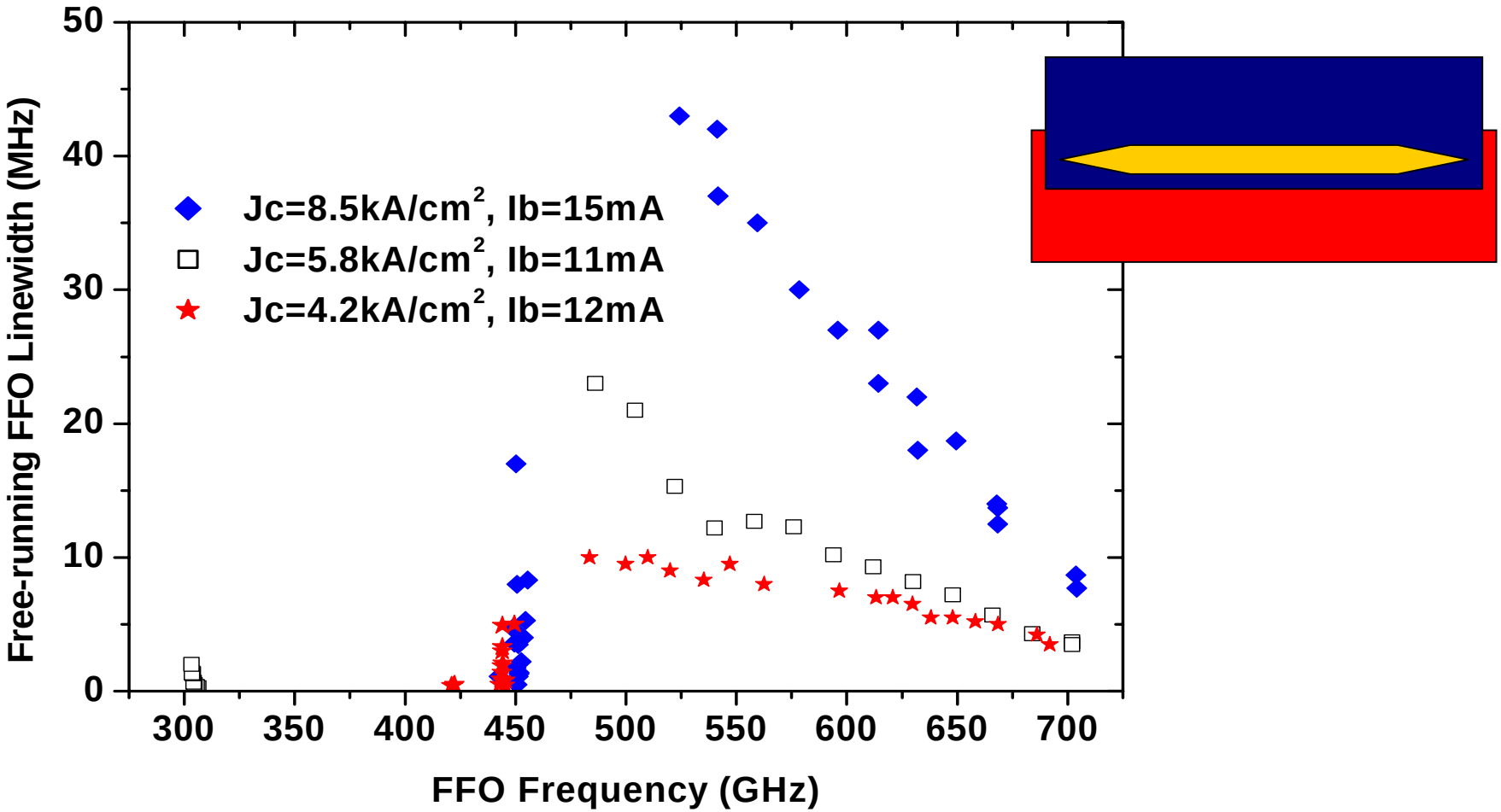
SIS Pumping by FFO (Different Designs)



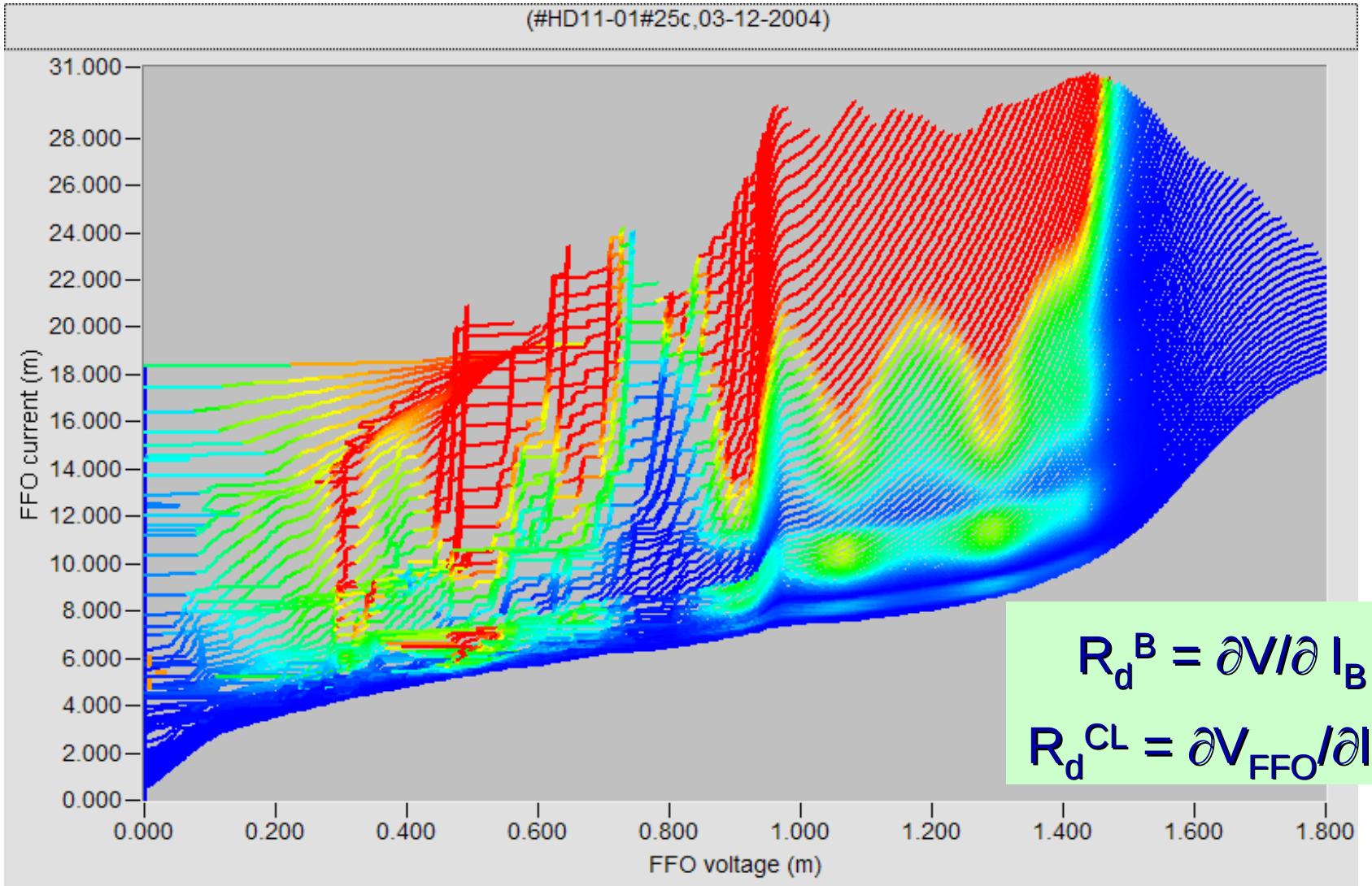
FFO Power
delivered to HM and SIS mixer

- **Analysis of the results for different FFO designs (including FFO used in T1), which were fabricated with various current density (RnS) has demonstrated that delivered to HM power depends both on FFO design and junctions' RnS.**
- **Reason of insufficient pumping for T1 circuits at high frequencies and high current density has been found.**
- **New designs for T2 have been developed and tested, these circuits demonstrate sufficient pumping from 250 to 700 GHz for RnS from 50 to 15 $\Omega^*\mu^2$.**

FFO Linewidth: Dependence on FFO Frequency and Current Density



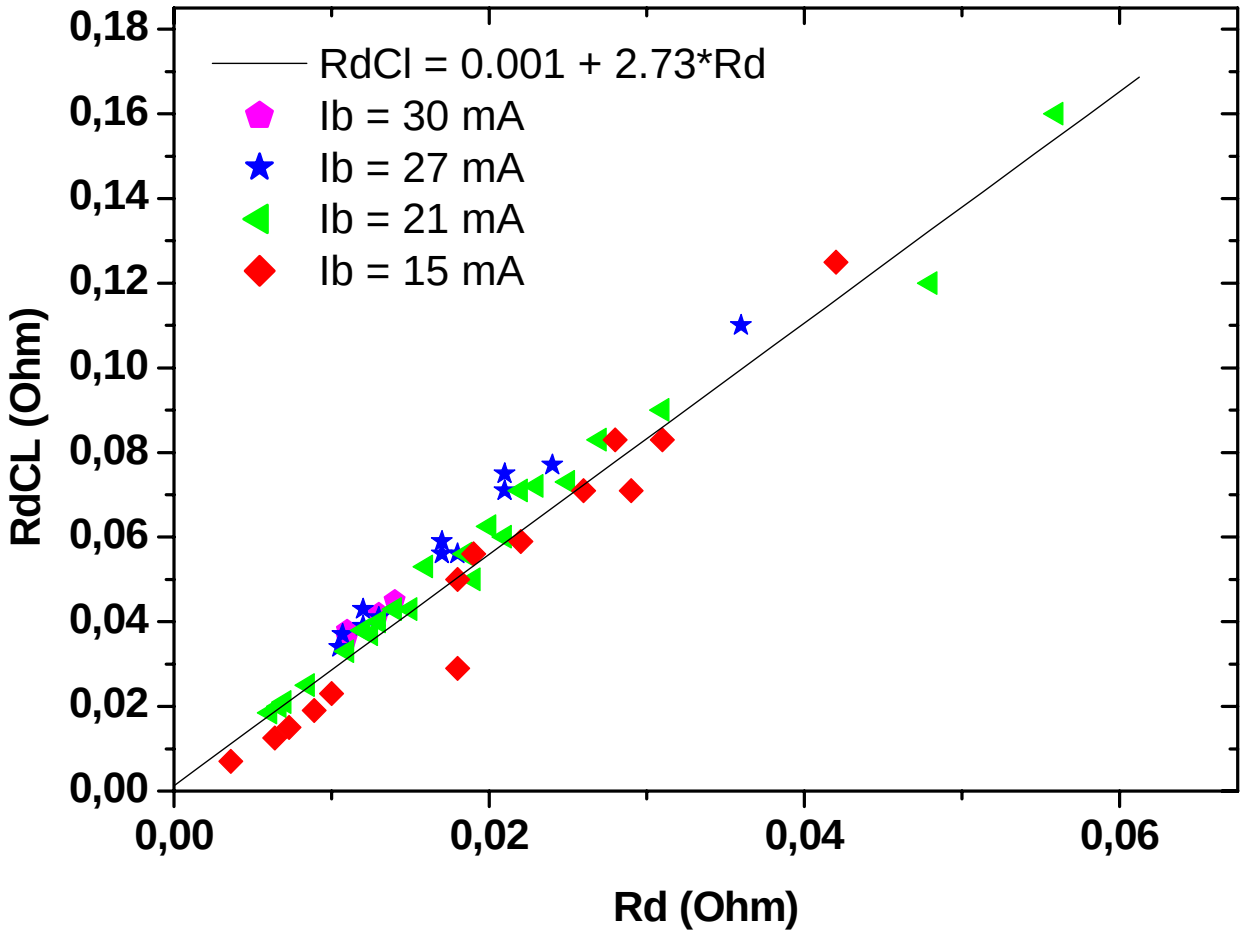
IVCs of FFO measured at different Icl



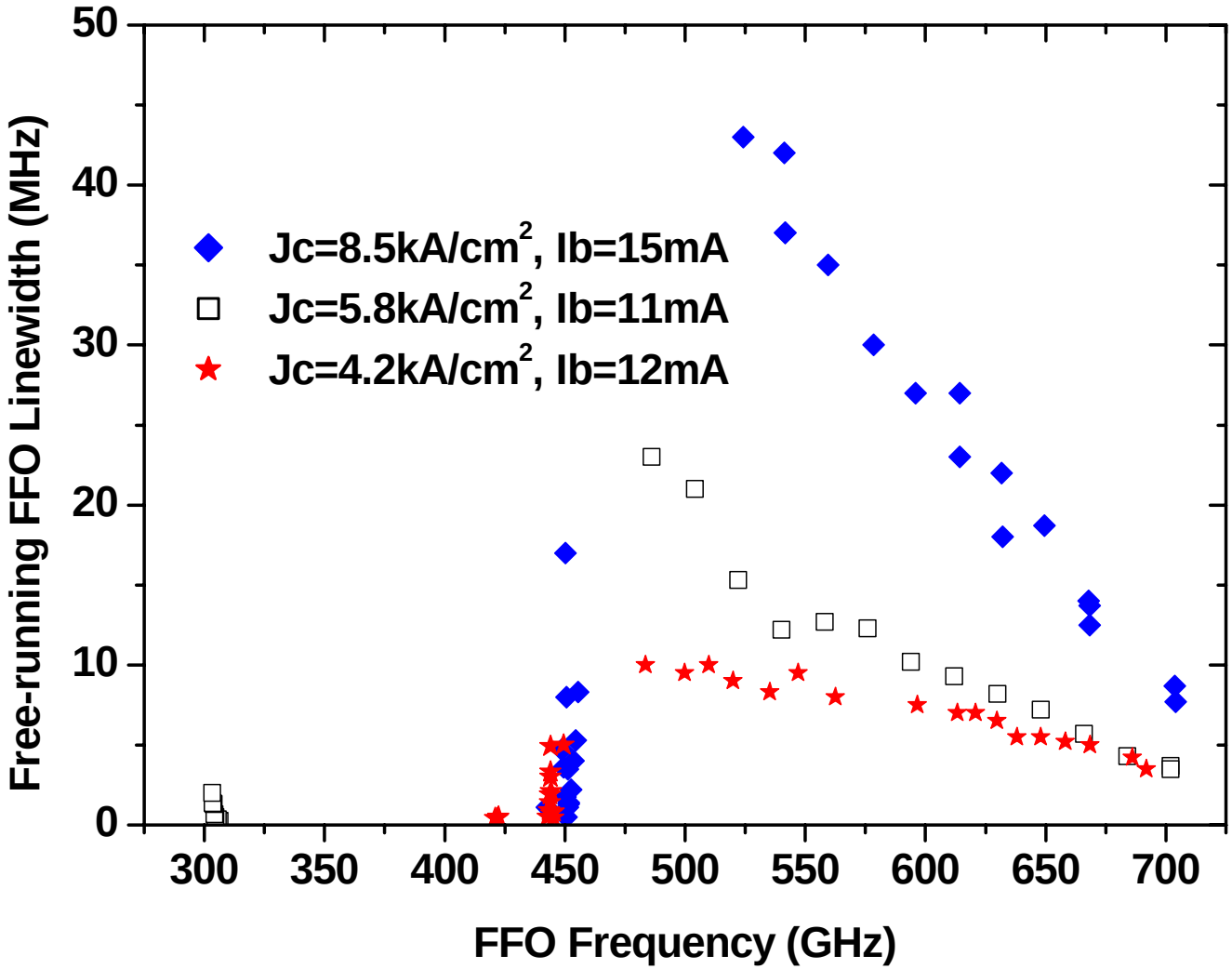
$R_d^B = \partial V / \partial I_B$

$R_d^{CL} = \partial V_{FFO} / \partial I_{CL}$

R_d^{CL} as a function of R_d

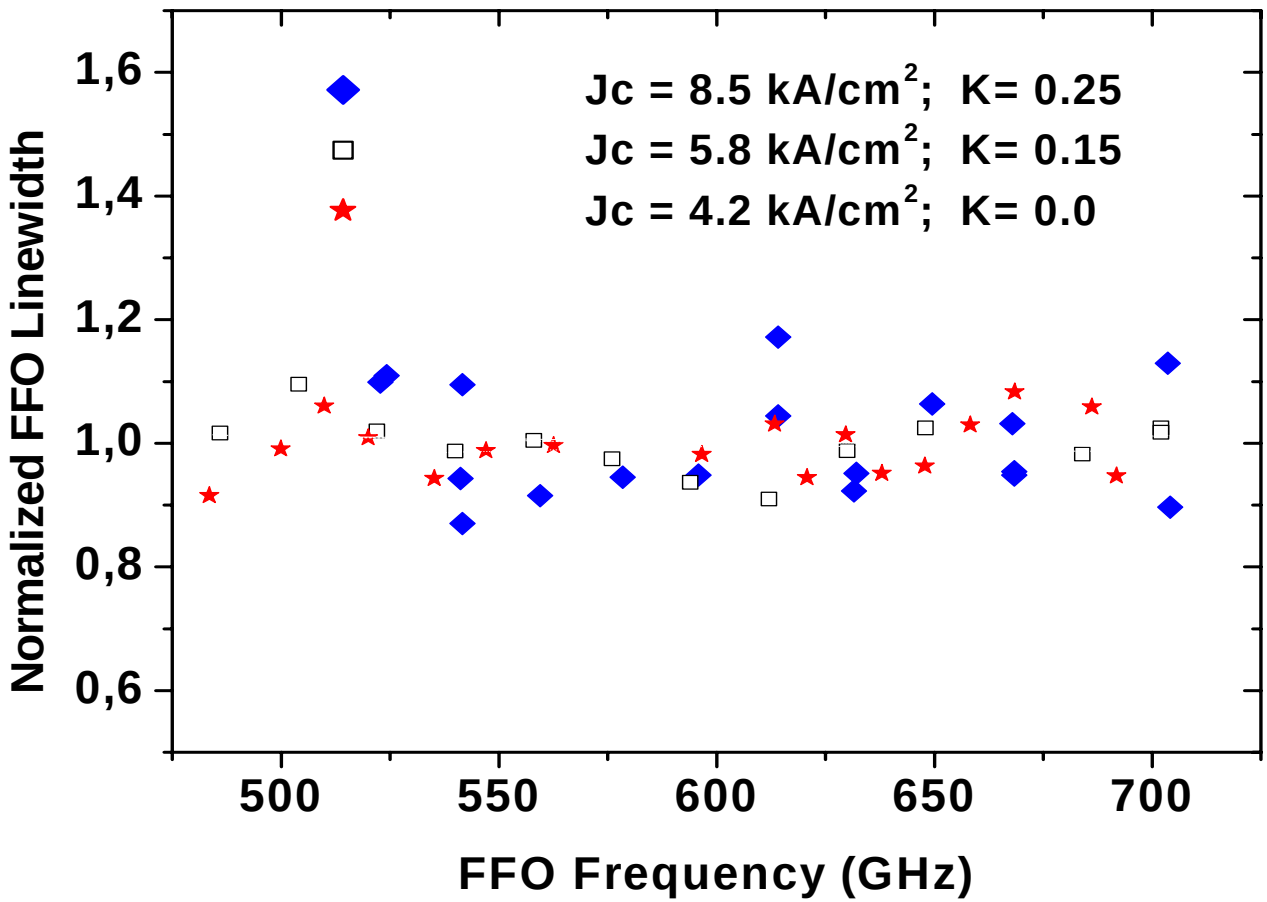


FFO Linewidth: Dependence on FFO Voltage and Current Density



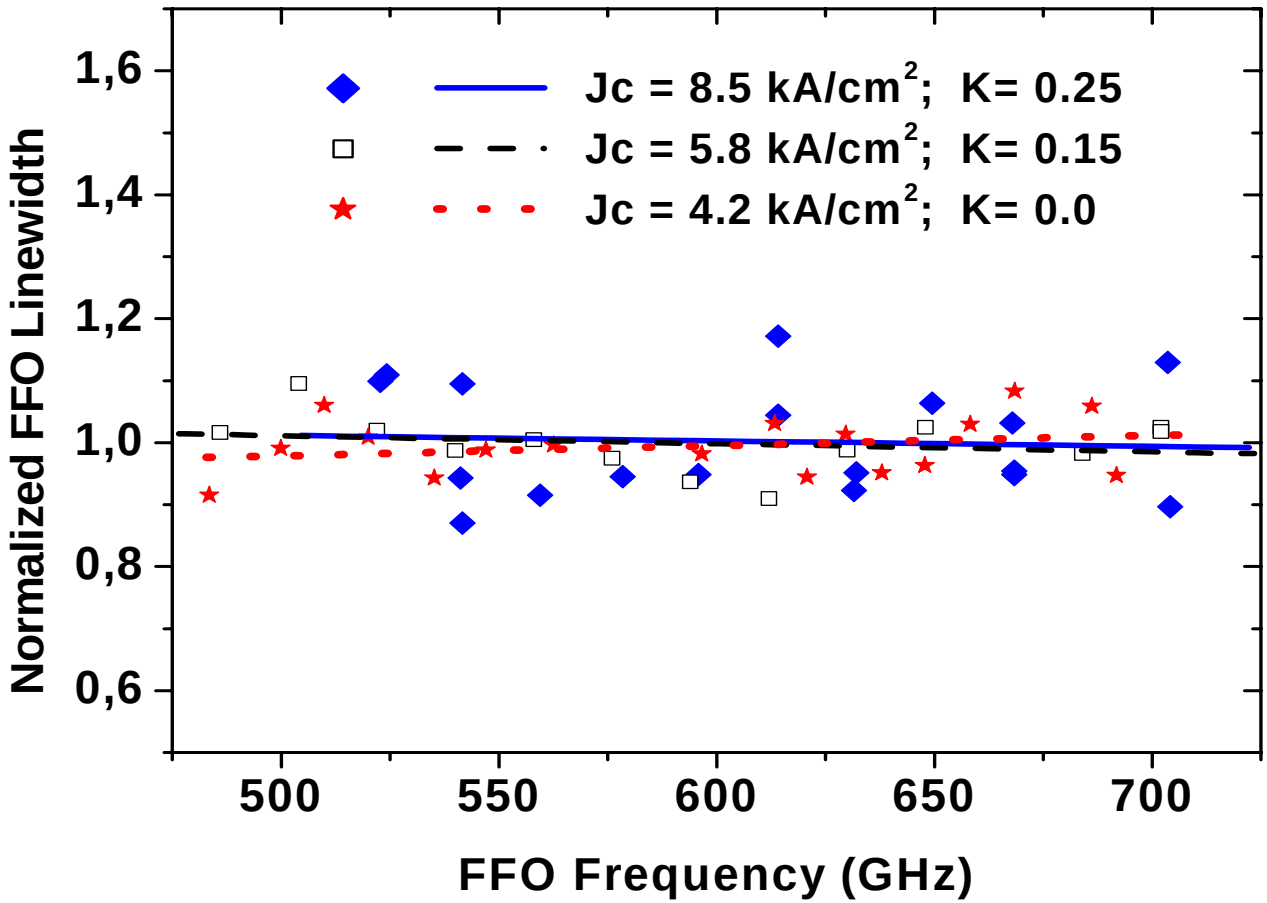
Normalized FFO Linewidth

$$\Delta f := \left(\frac{2\cdot e}{h}\right)^2 \cdot \left(R_d + K\cdot R_{dCL}\right)^2 \cdot \left[\frac{e\cdot(Iqp)}{2\cdot\pi}\cdot\coth\left(\frac{e\cdot V}{2\cdot k_b\cdot T}\right) + \frac{2\cdot e\cdot(Is)}{2\cdot\pi}\cdot\coth\left(\frac{e\cdot V}{k_b\cdot T}\right)\right] + \frac{1}{\pi}\cdot\left(\frac{2\cdot e}{h}\right)\cdot\left(R_d + R_{dCL}\right)\cdot I_{If}$$

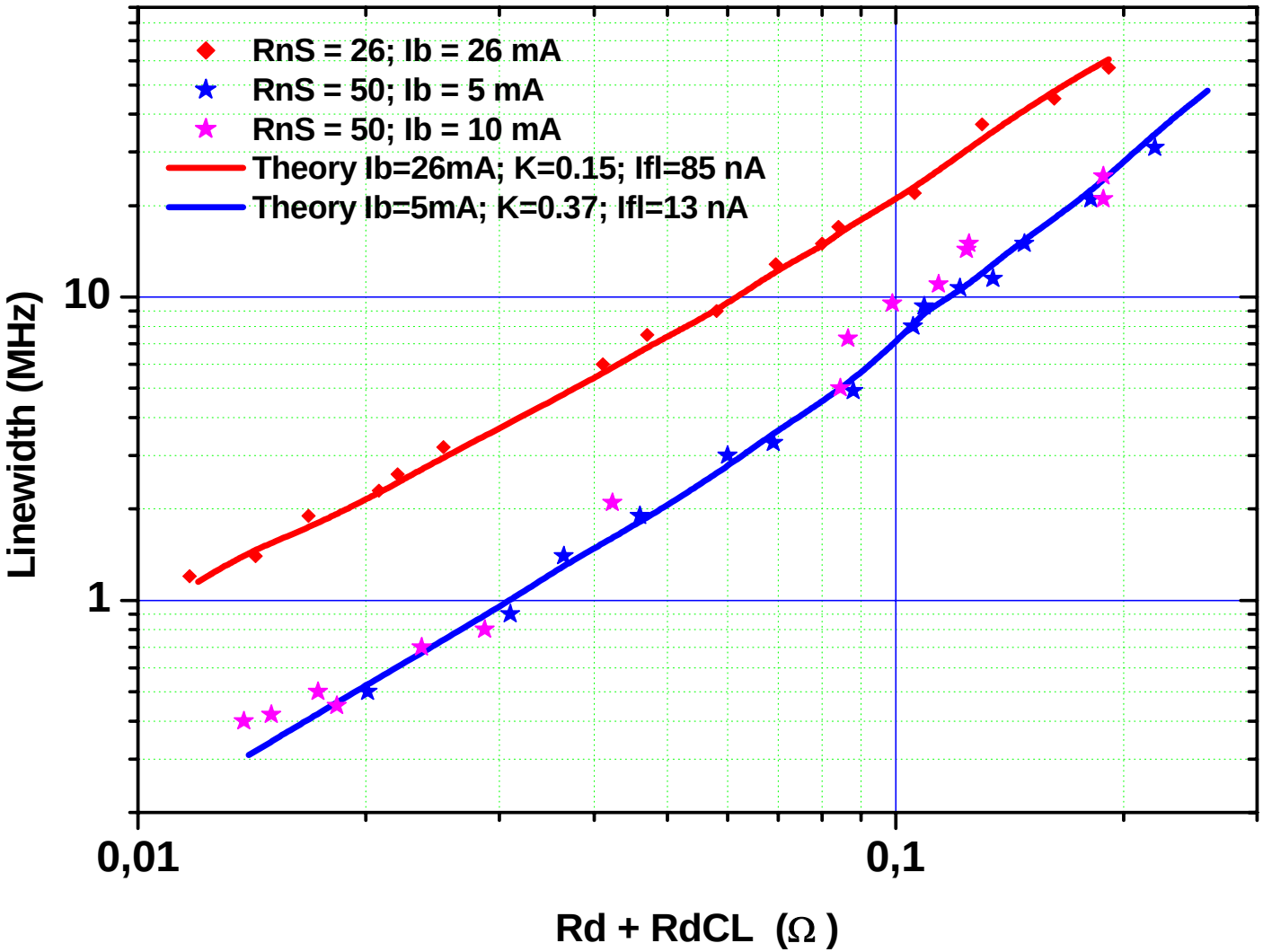


Normalized FFO Linewidth

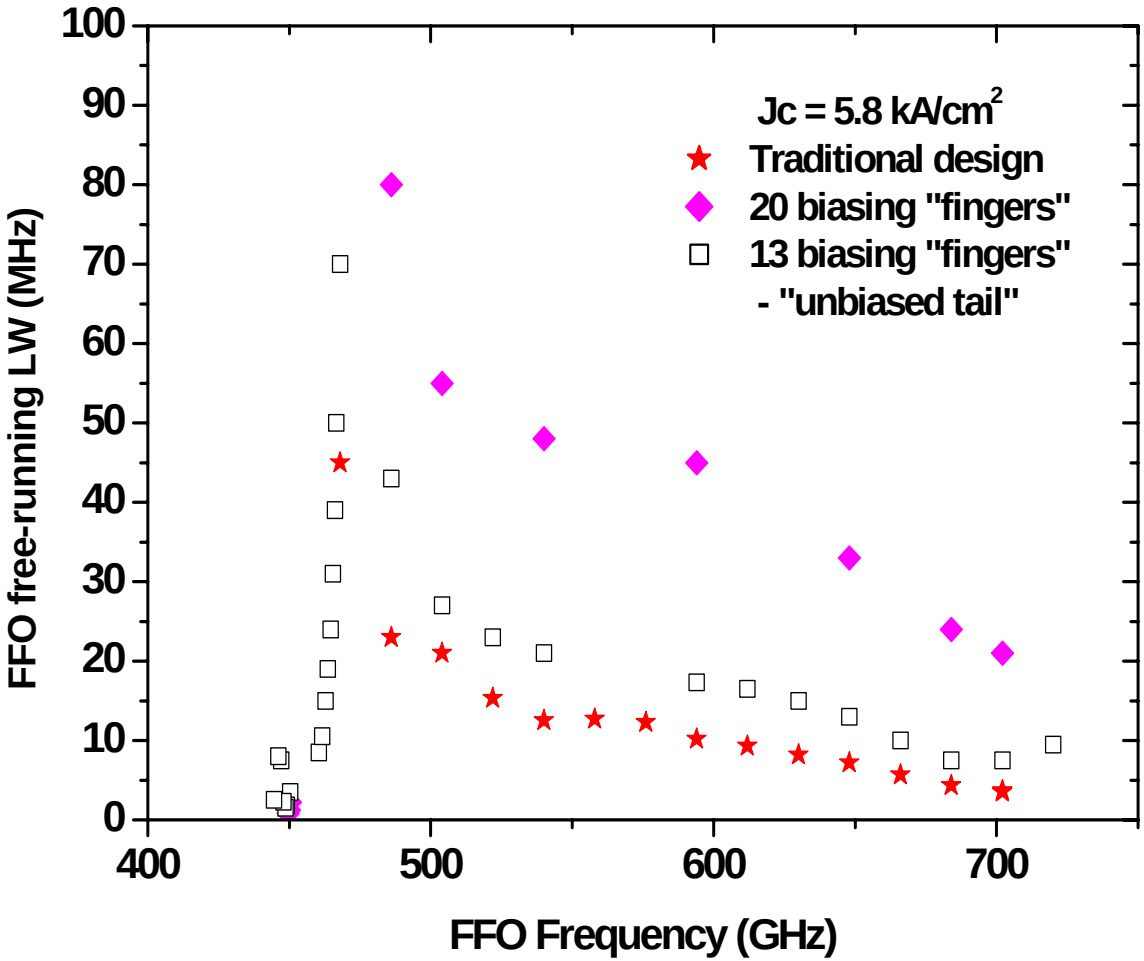
$$\Delta f := \left(\frac{2\cdot e}{h}\right)^2 \cdot \left(R_d + K\cdot R_{dCL}\right)^2 \cdot \left[\frac{e\cdot(Iqp)}{2\cdot\pi}\cdot\coth\left(\frac{e\cdot V}{2\cdot k_b\cdot T}\right) + \frac{2\cdot e\cdot(Is)}{2\cdot\pi}\cdot\coth\left(\frac{e\cdot V}{k_b\cdot T}\right)\right] + \frac{1}{\pi}\cdot\left(\frac{2\cdot e}{h}\right)\cdot\left(R_d + R_{dCL}\right)\cdot I_{If}$$

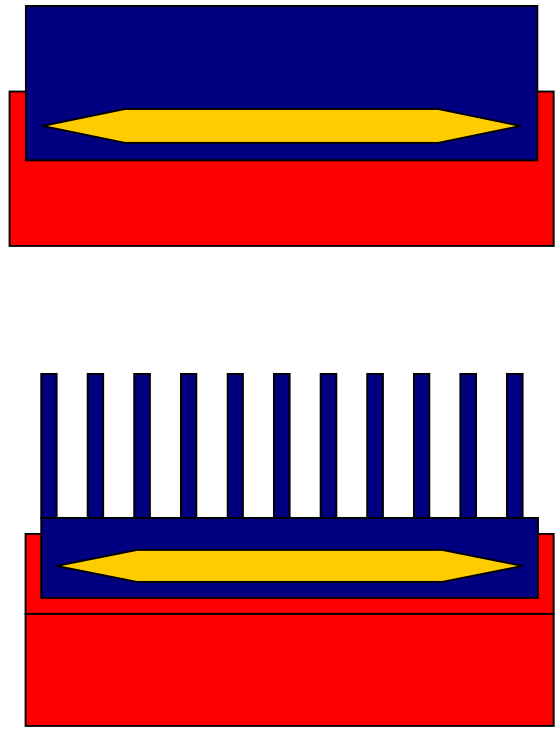


FFO Linewidth on ($R_d + R_d^{CL}$)

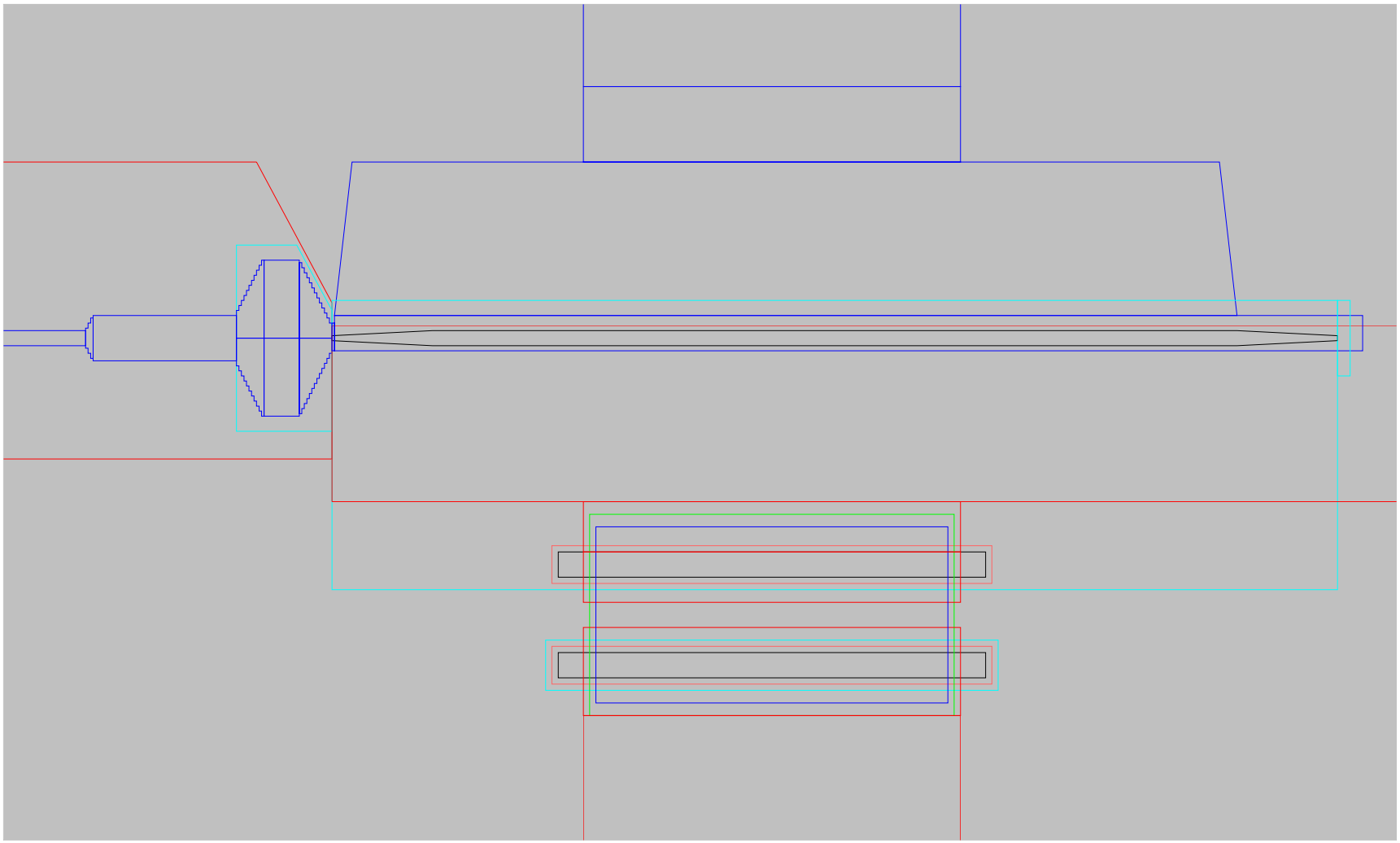


FFO Linewidth (Design issue)

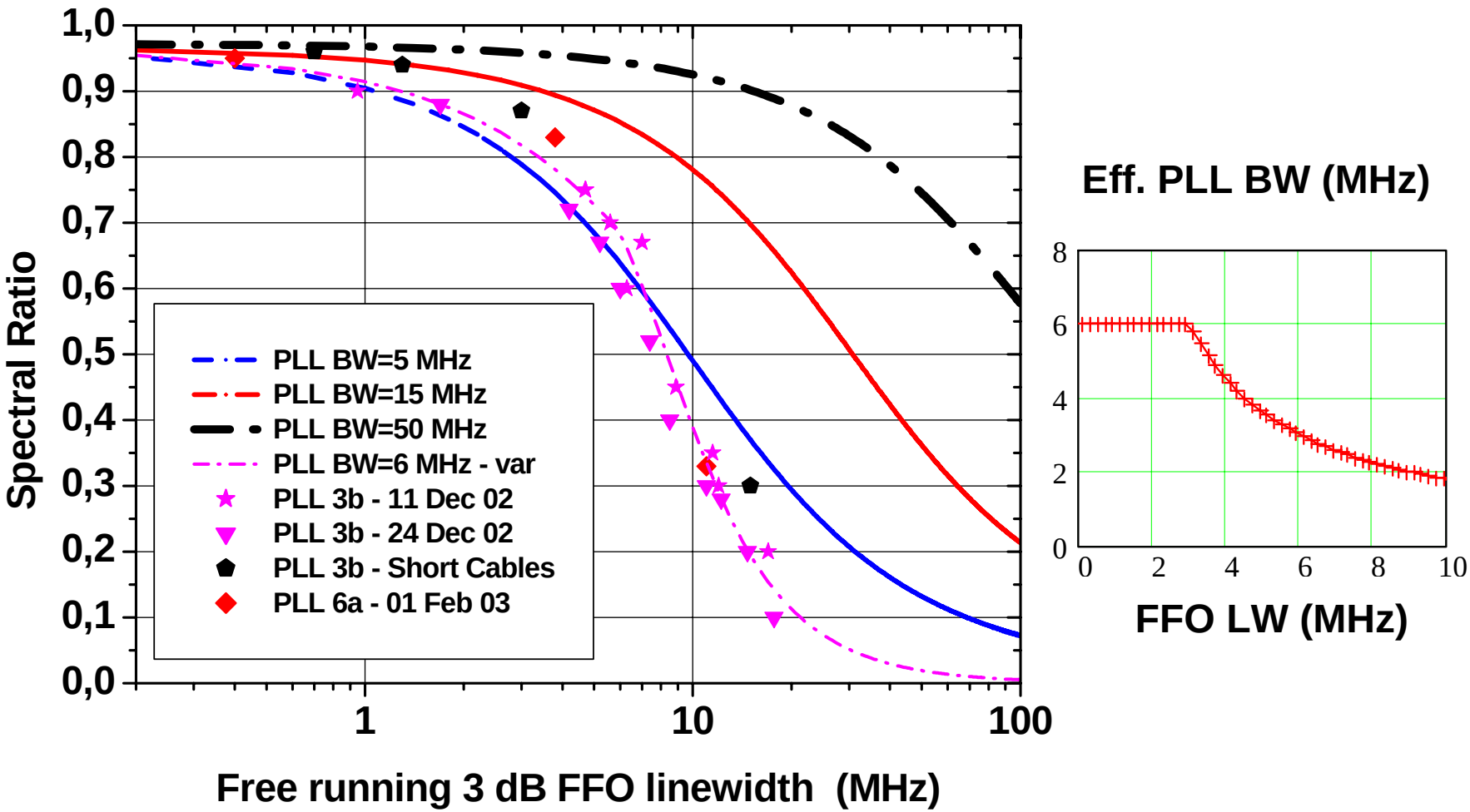




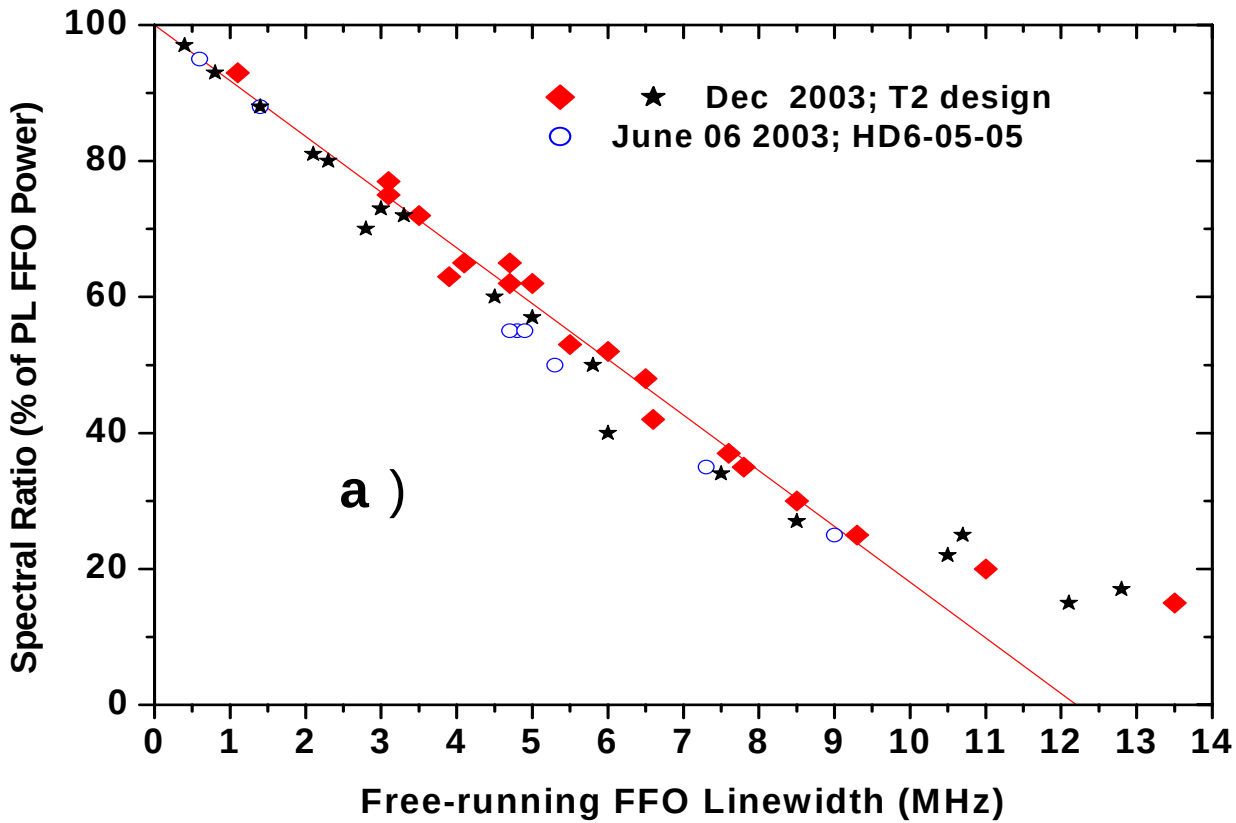
FFO of T2 design with unbiased tail



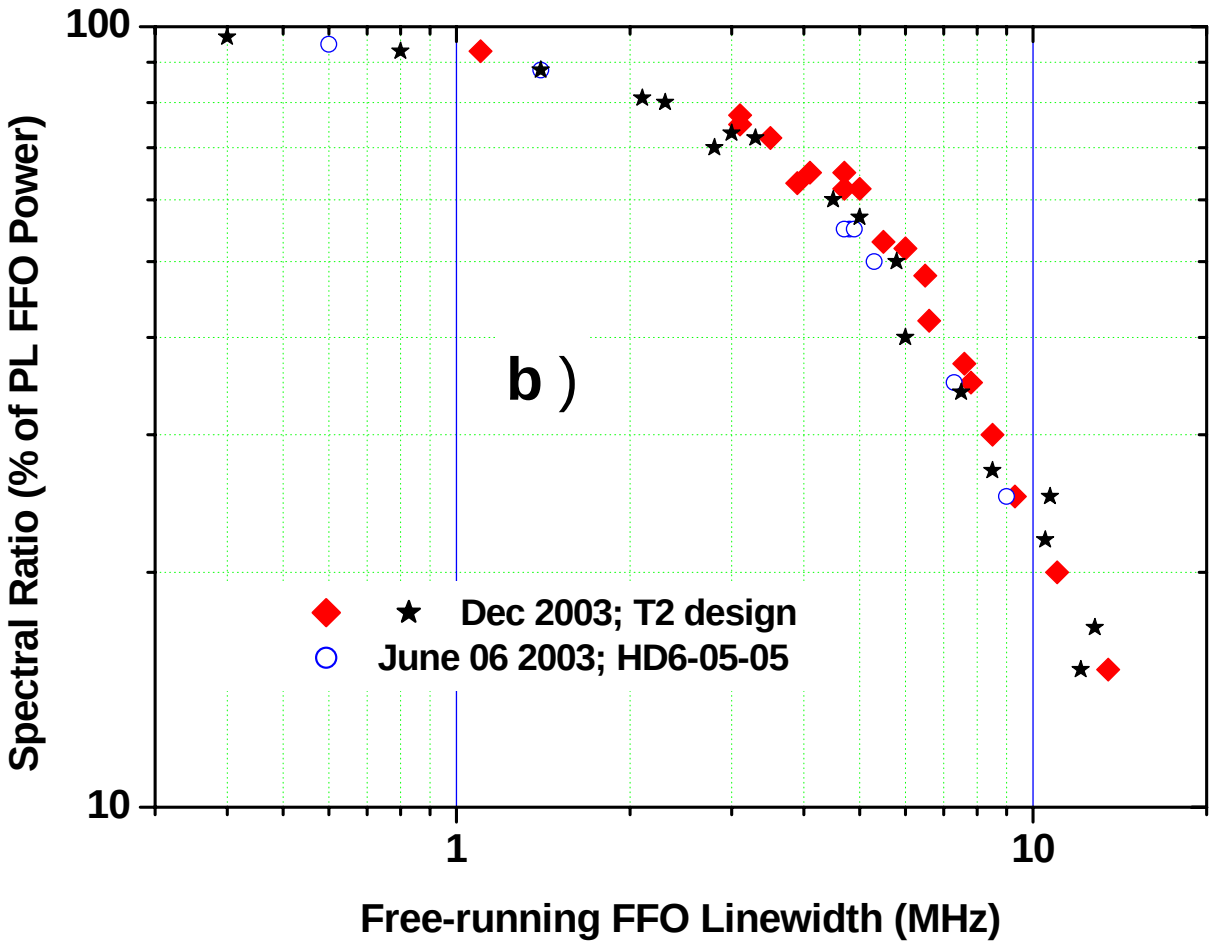
Ratio of PL and total FFO power



Spectral Ratio of the PL FFO vs free running FFO linewidth

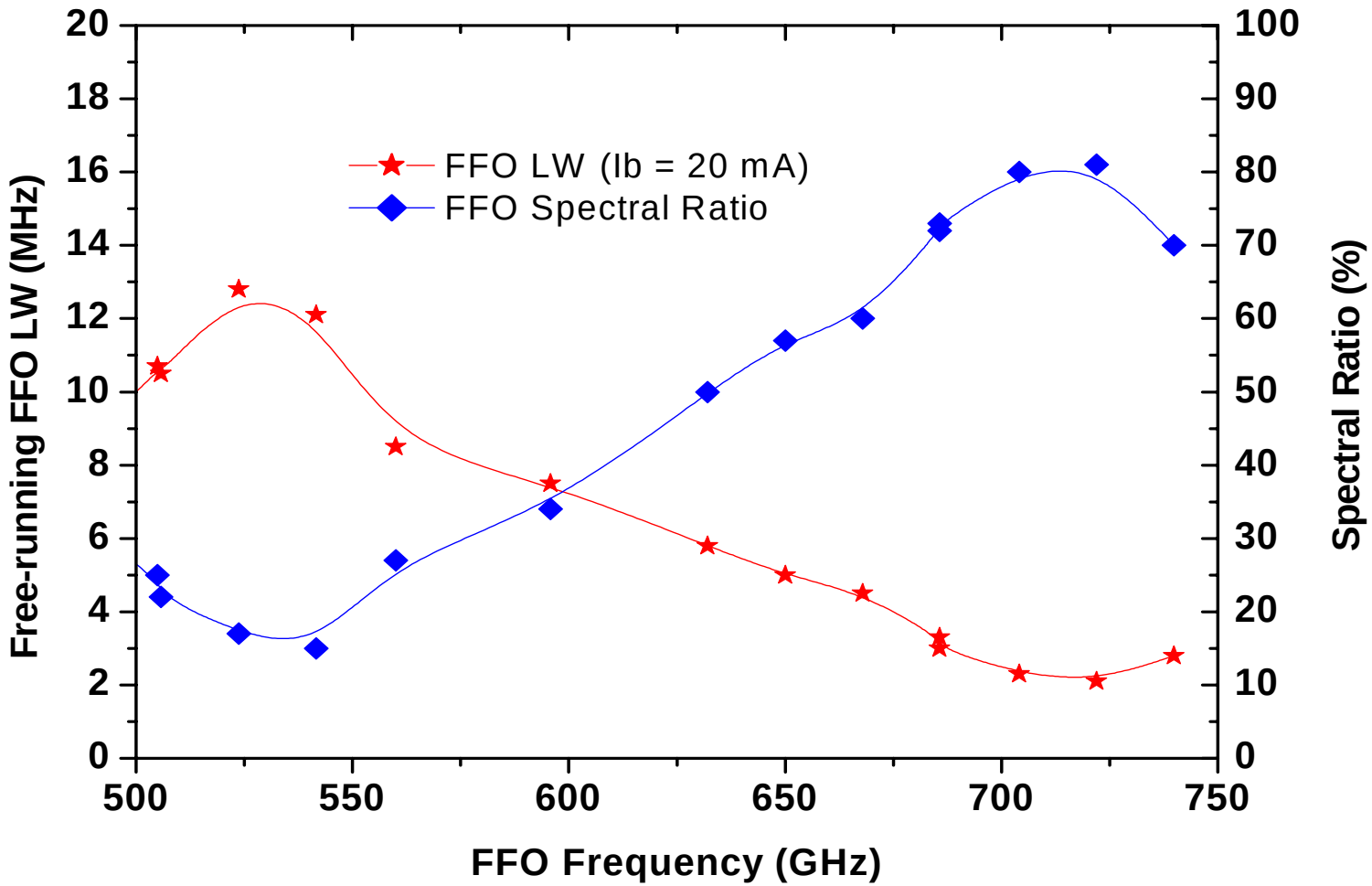


Spectral Ratio of the PL FFO vs free running FFO linewidth

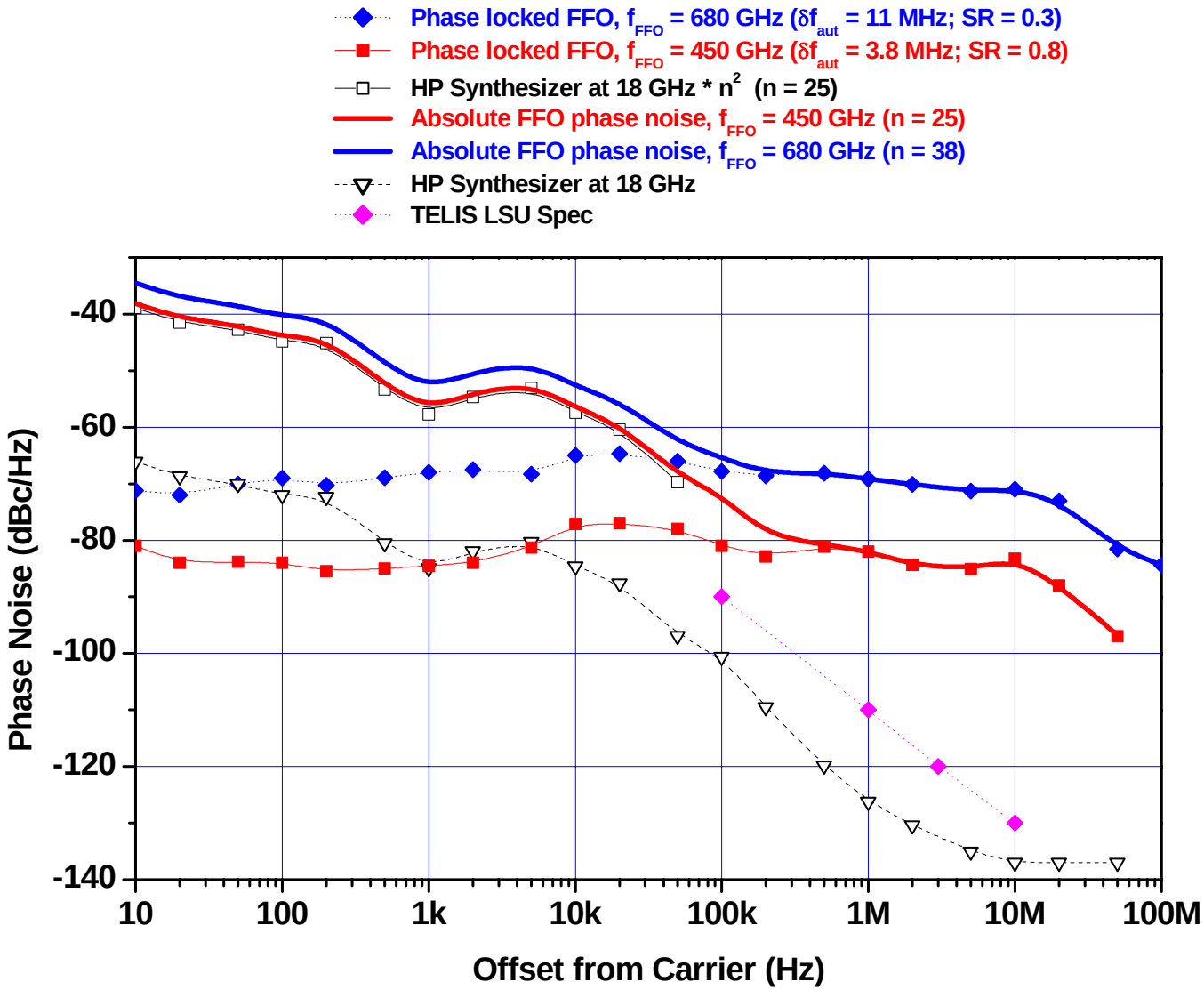


FFO LW and SR vs FFO frequency

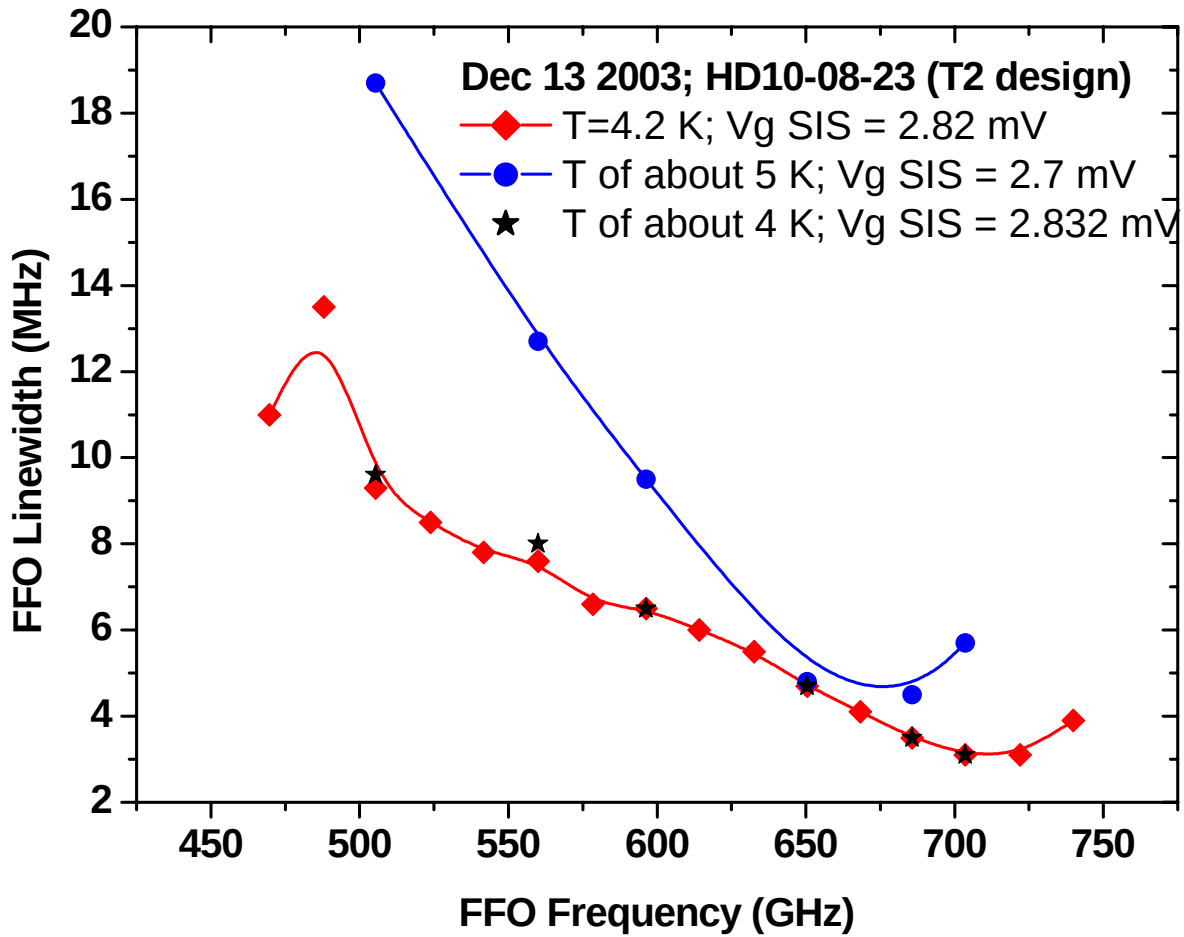
(W_{FFO} = 10 μ; RnS = 40 Ω*μ²)



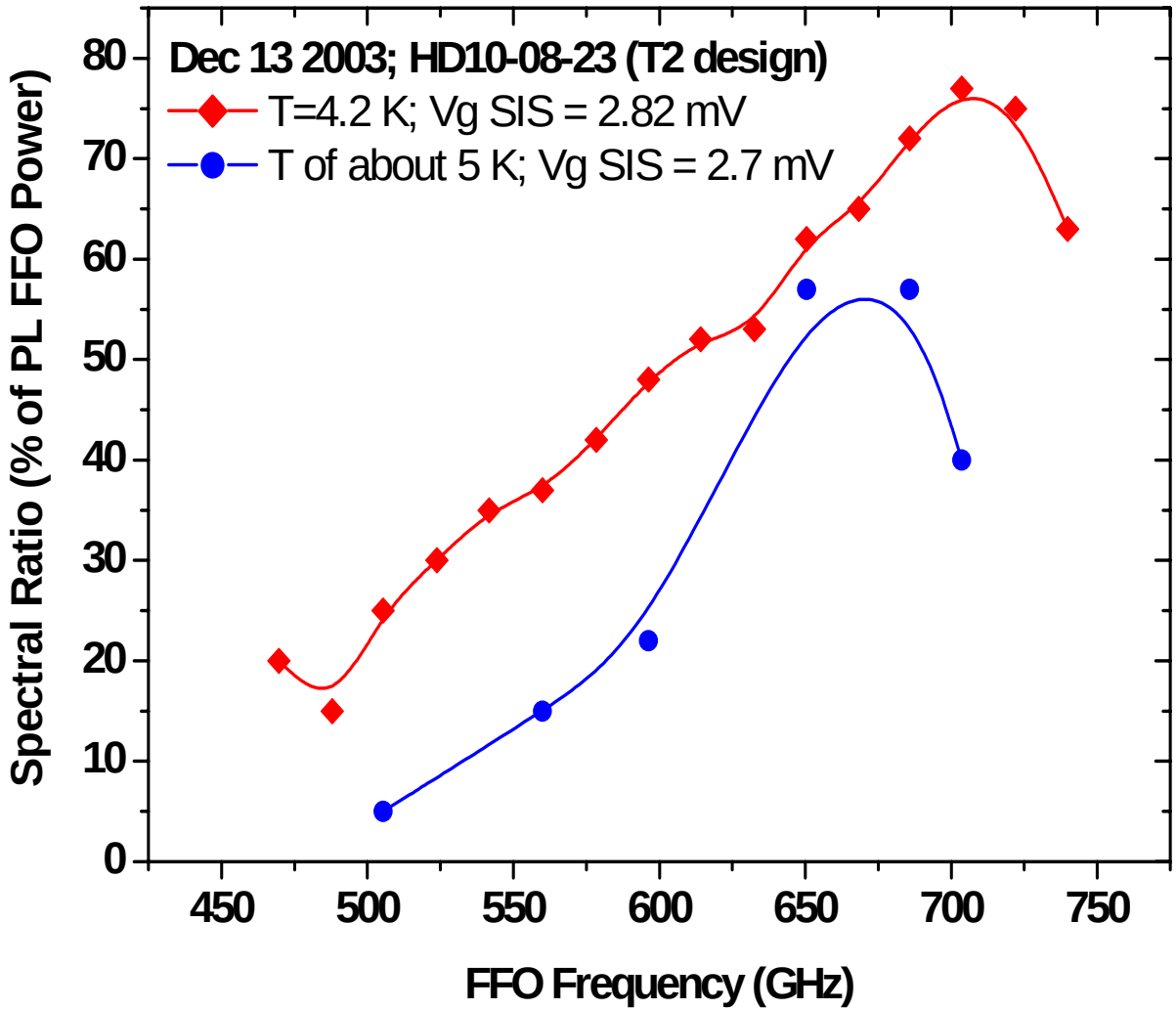
Phase Noise of the PL FFO (Breadboard)



FFO linewidth vs FFO frequency, measured at different temperatures



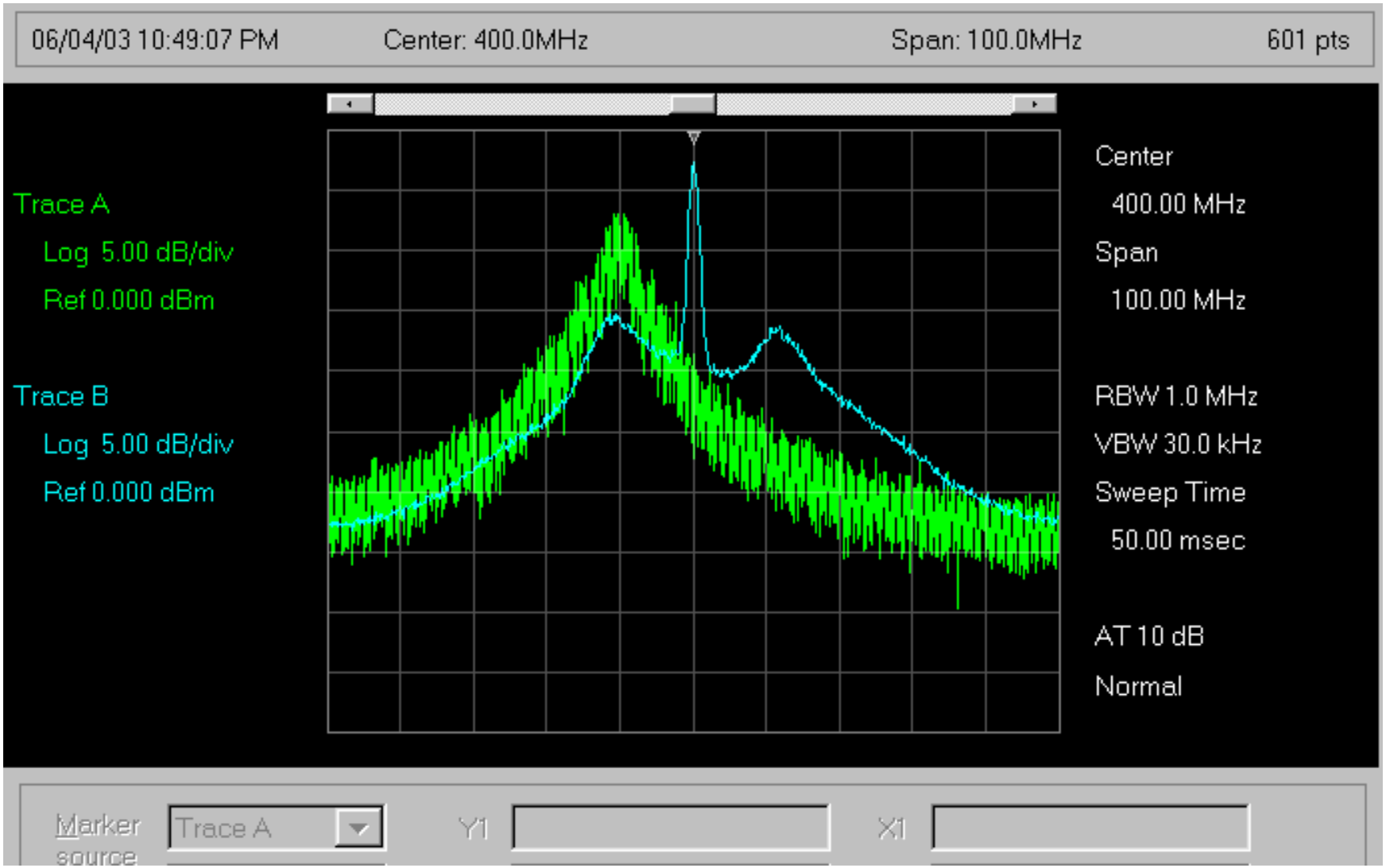
Spectral Ratio of the PL FFO vs frequency, measured at different temperatures



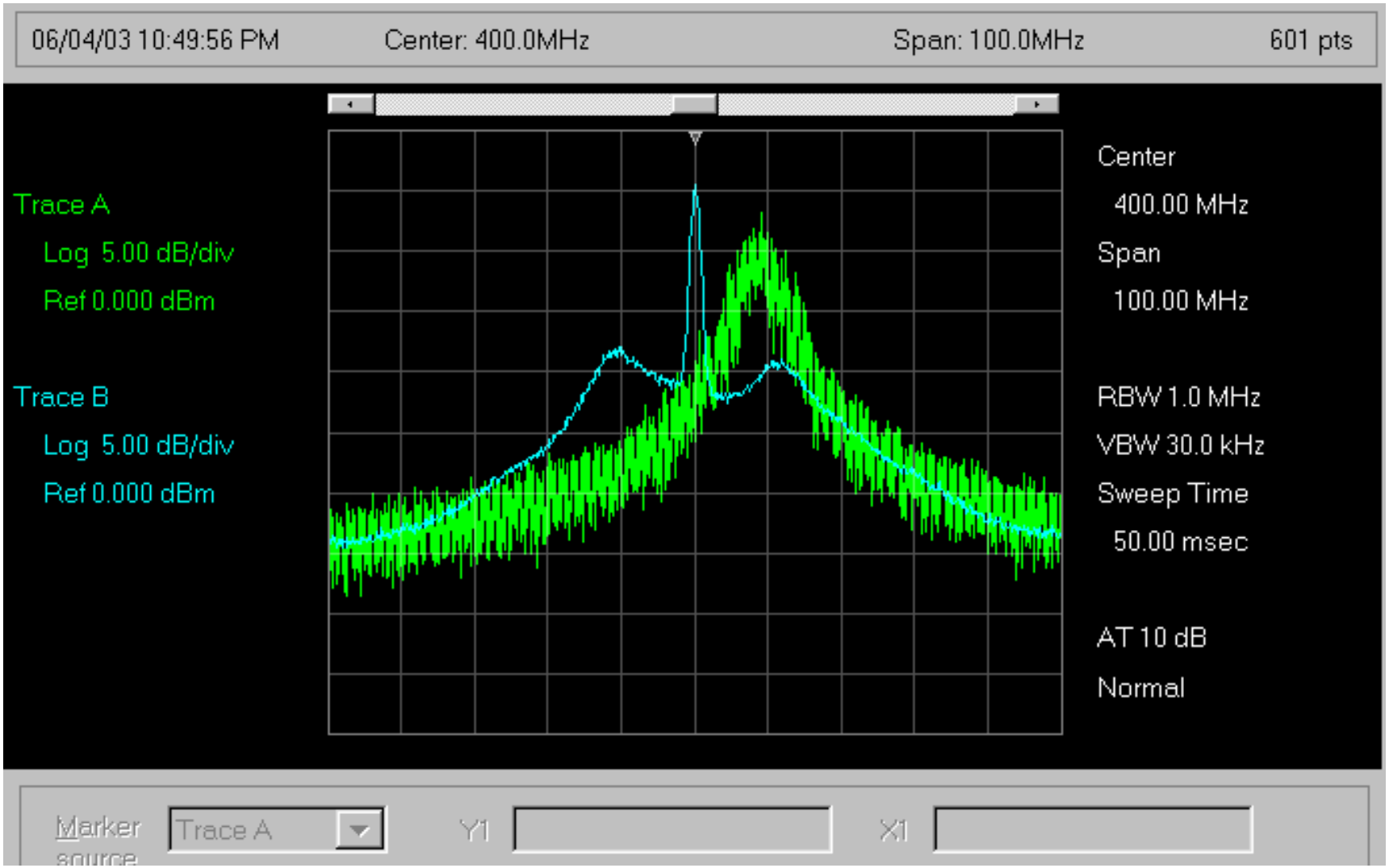
FFO Shielding

- **Superconducting shield: stability of the PL FFO at changing of dewar orientation.**
- **Magnetic / Superconducting shield combination: reproducibility of the FFO state after heating.**

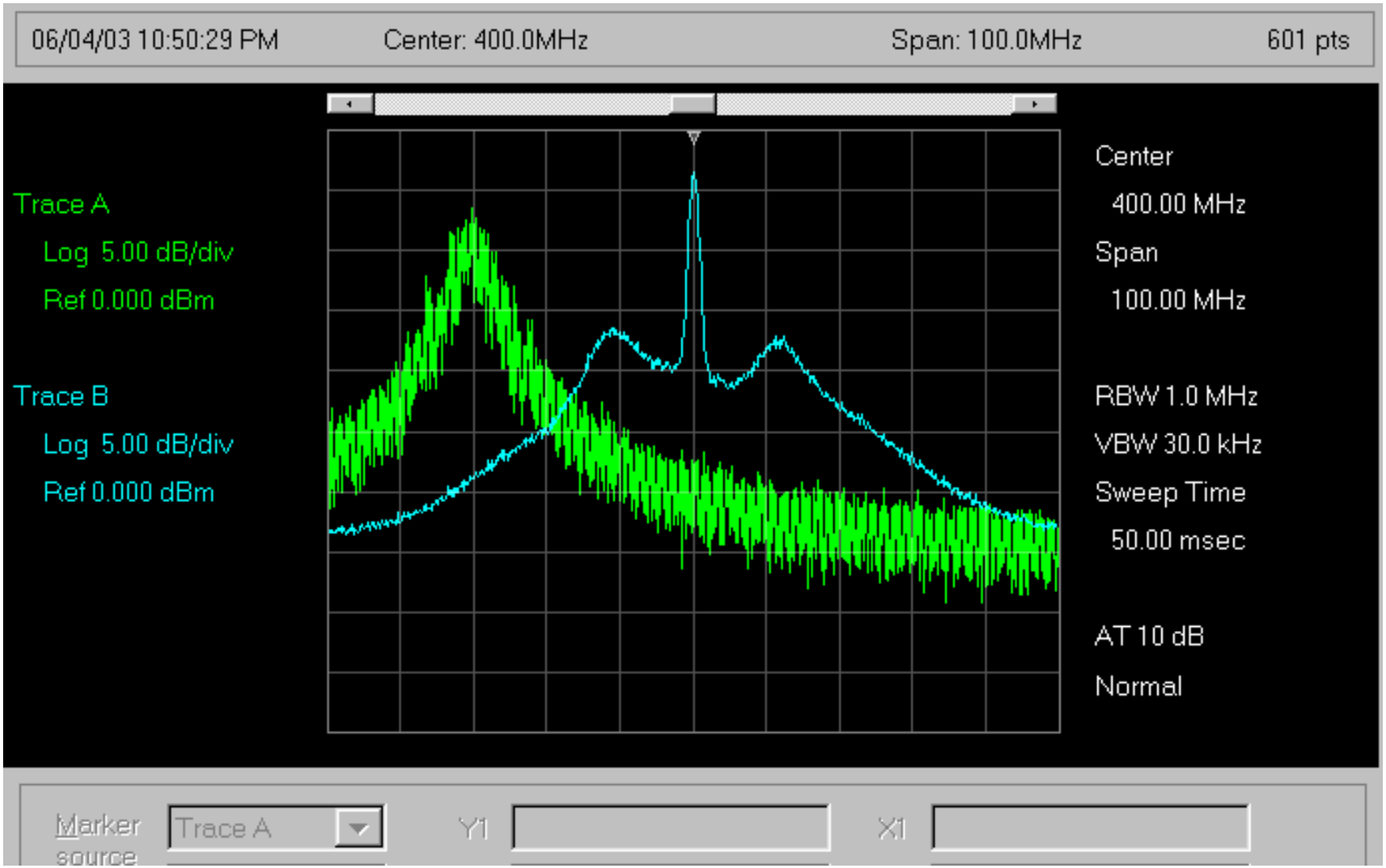
Free-running and PL FFO Spectra; f FFO = 687 GHz



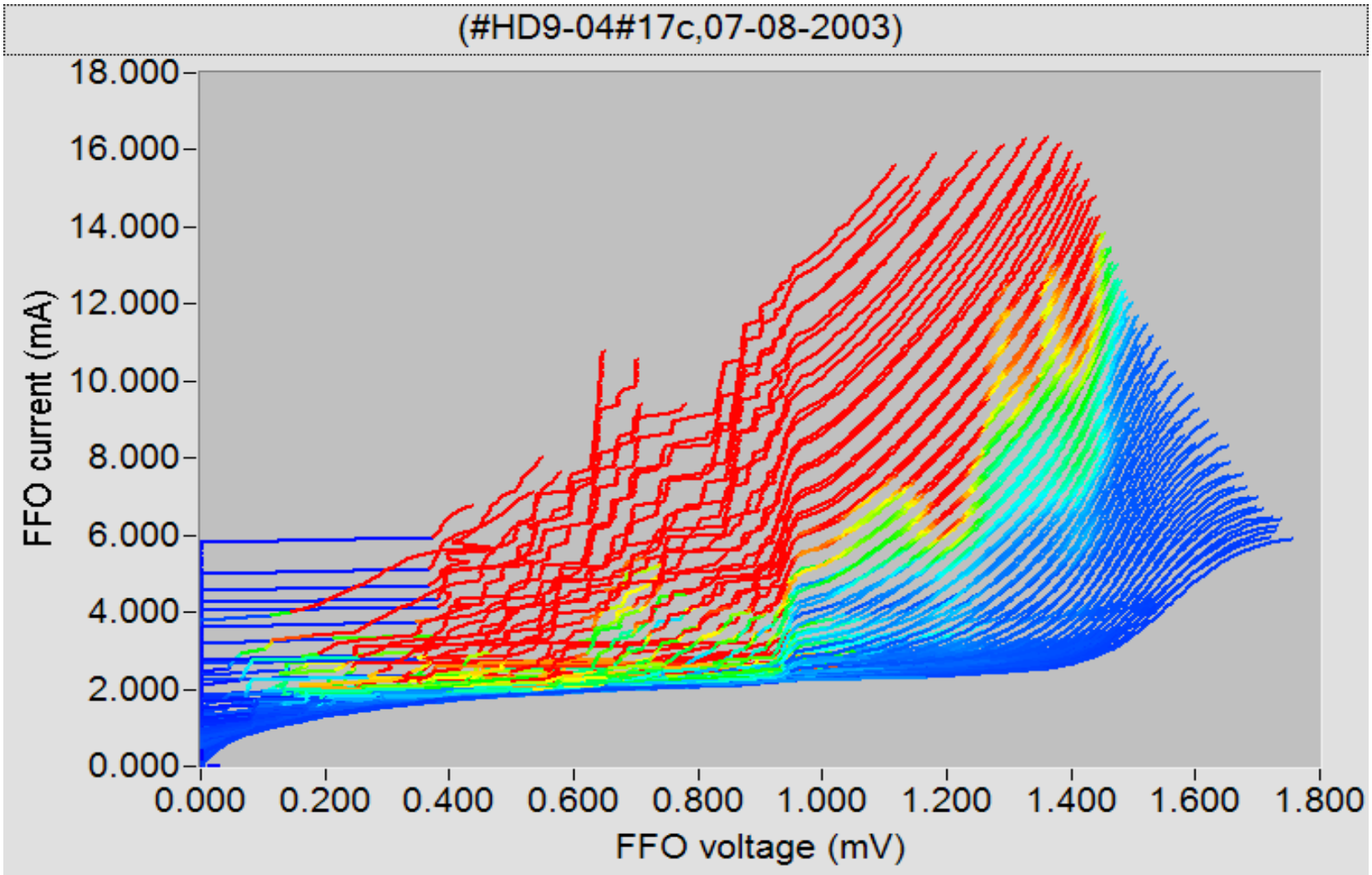
Free-running and PL FFO Spectra, dewar rotated on 90 deg



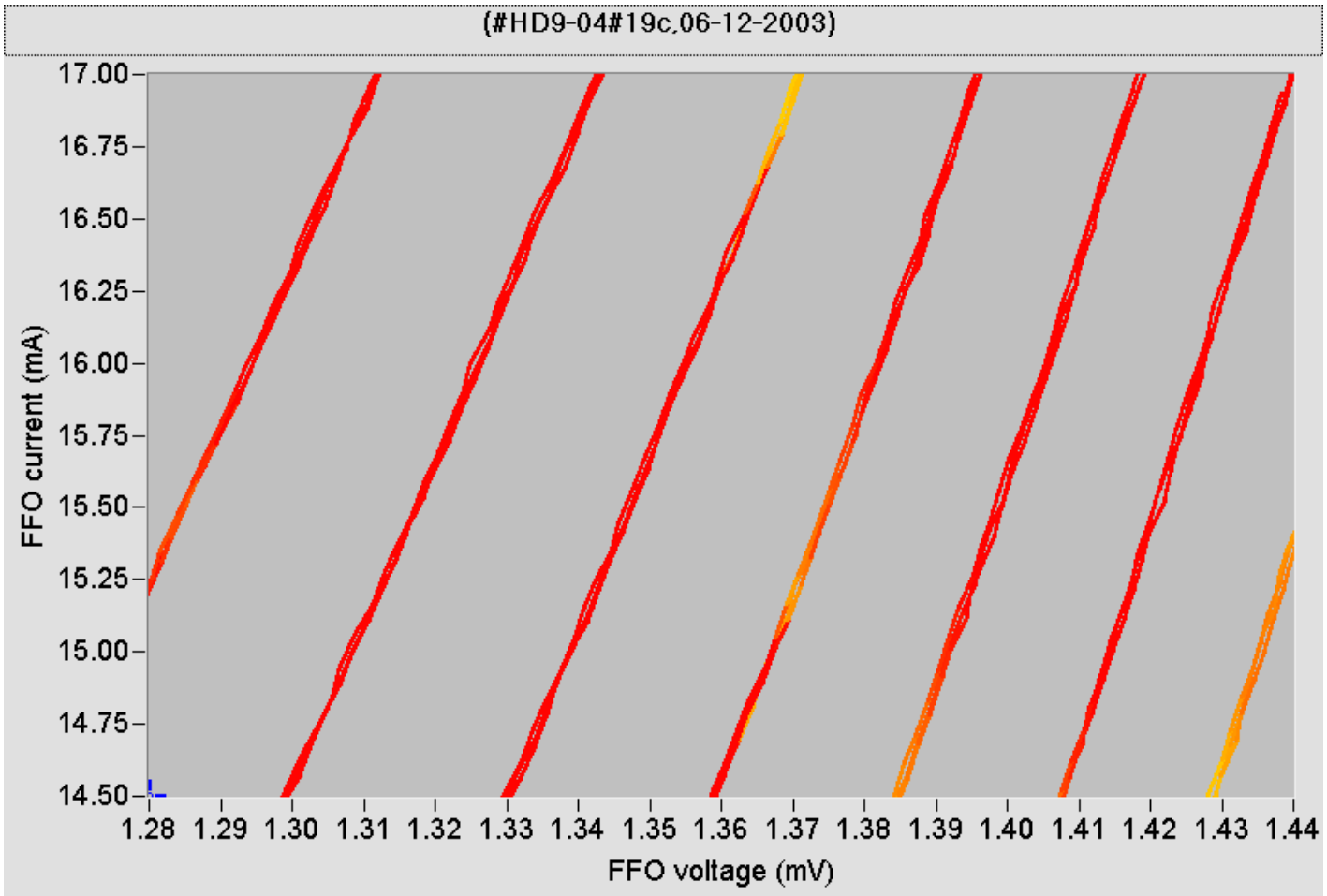
Free-running and PL FFO spectra, dewar rotated on - 90 deg



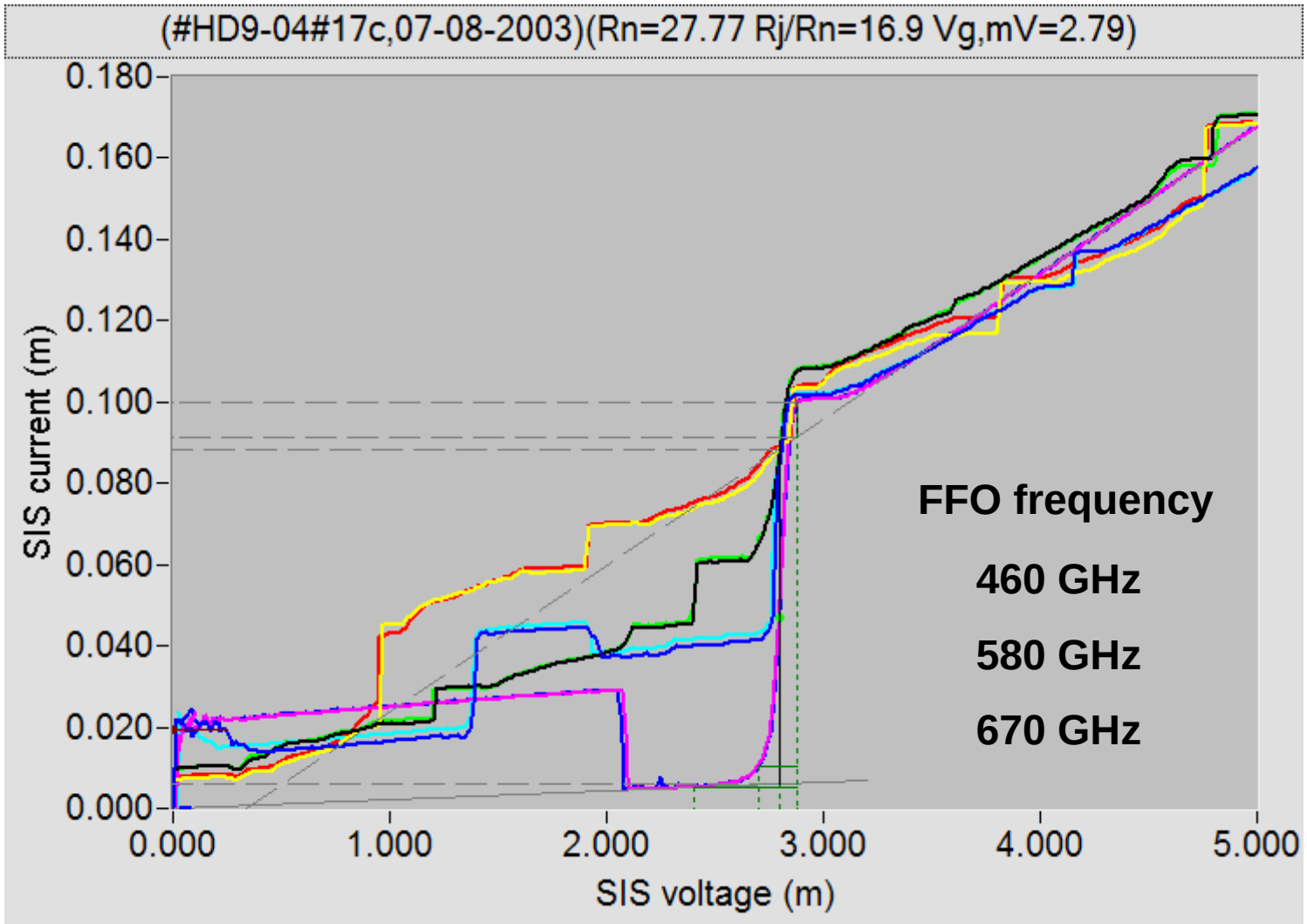
FFO IVCs measured after 2 consequent thermocyclings ('usual" situation – there is a shift of about 100 μV)



Part of the FFO IVCs measured after 3 consequent thermocyclings ('perfect" situation – shift is of about 1 μV)

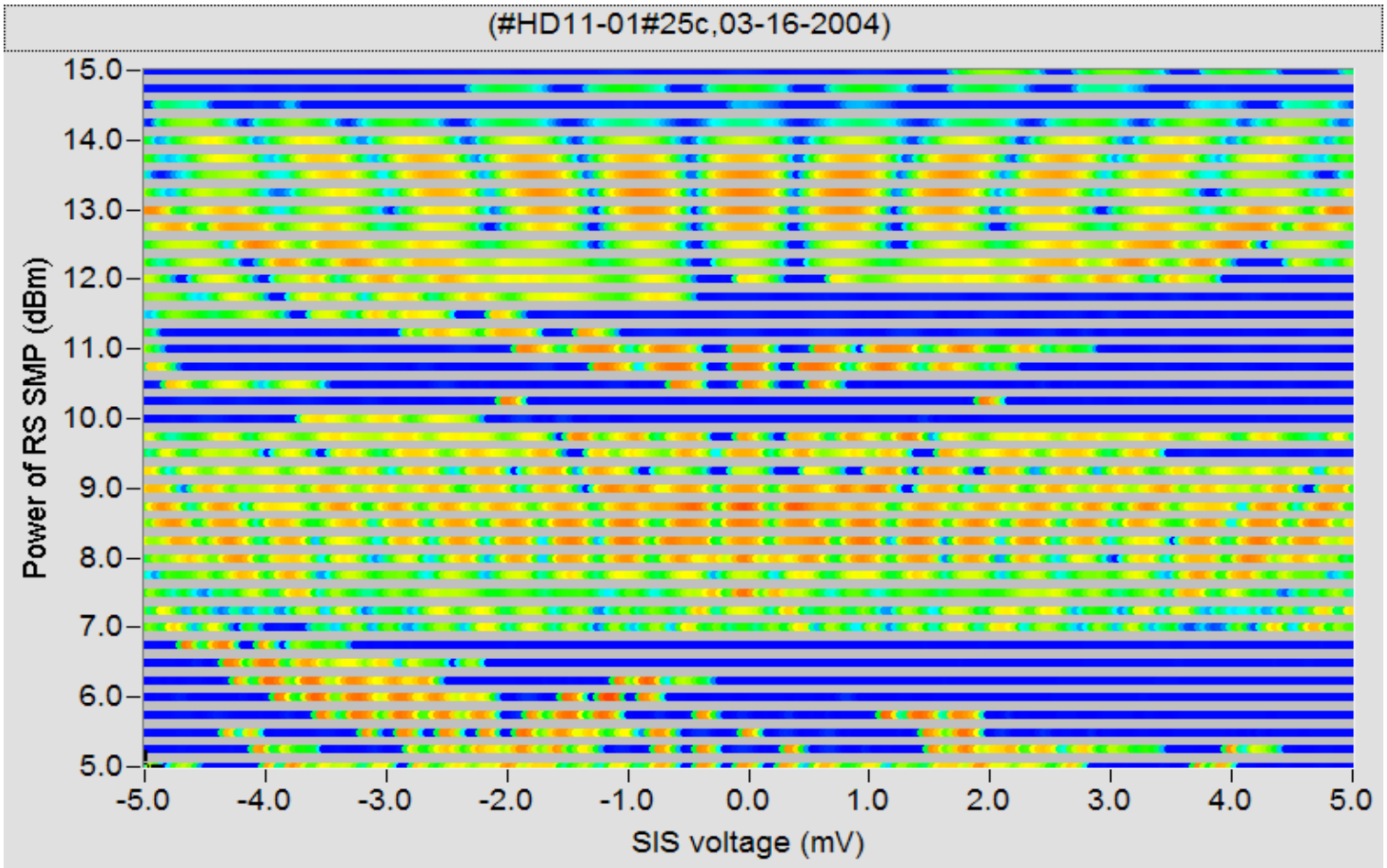


SIS IVCs pumped by FFO measured after 2 consequent thermocyclings

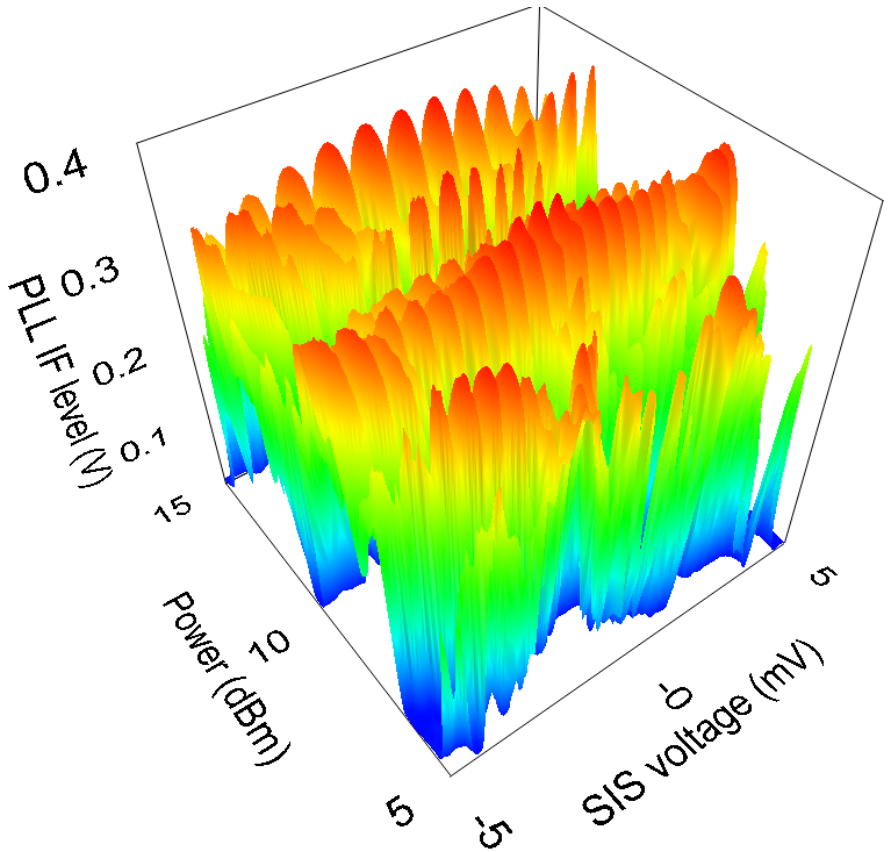


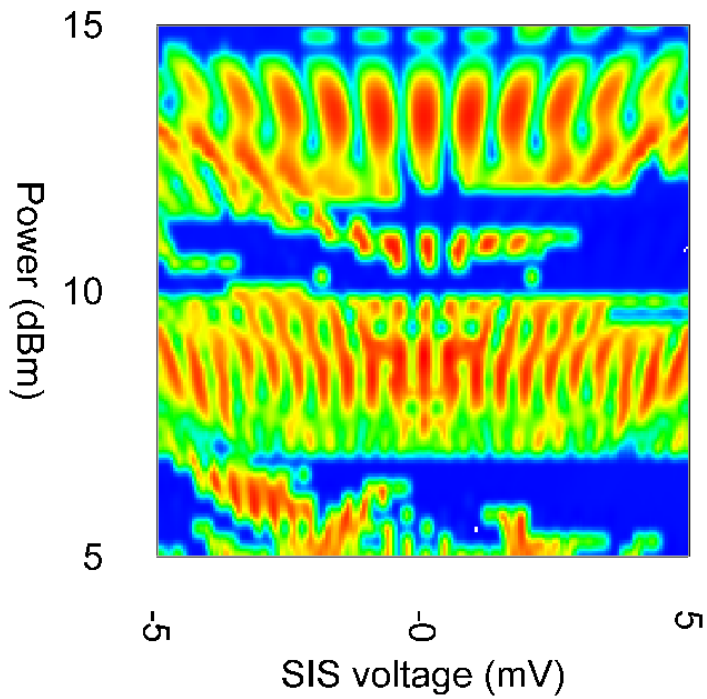
2-D diagram for HM operational parameters measured by PC controlled PLL.

The color represents the IF-out PLL signal.

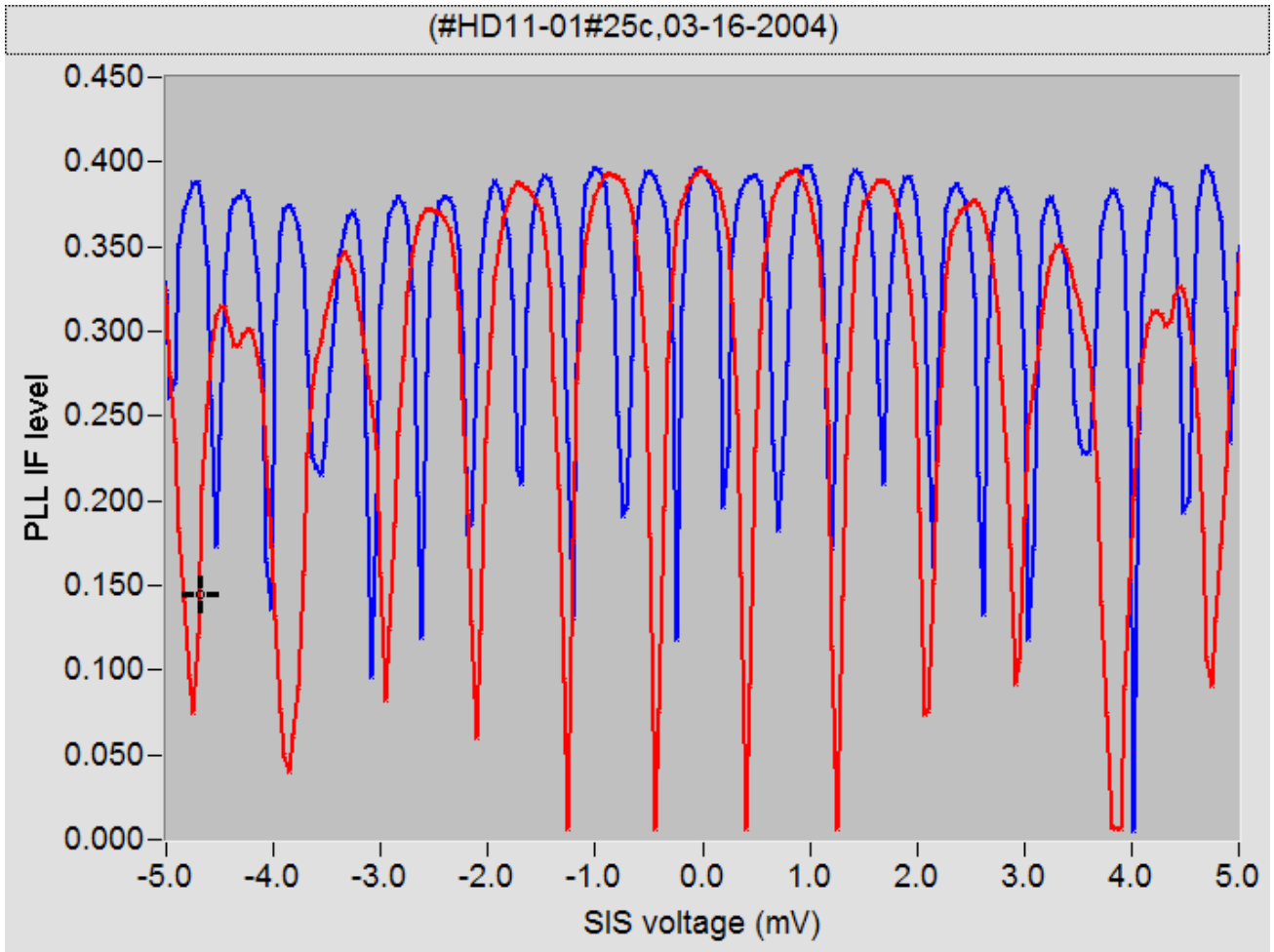


3-D diagram for HM operational parameters measured by PC controlled PLL.
The color represents the IF-out PLL signal.

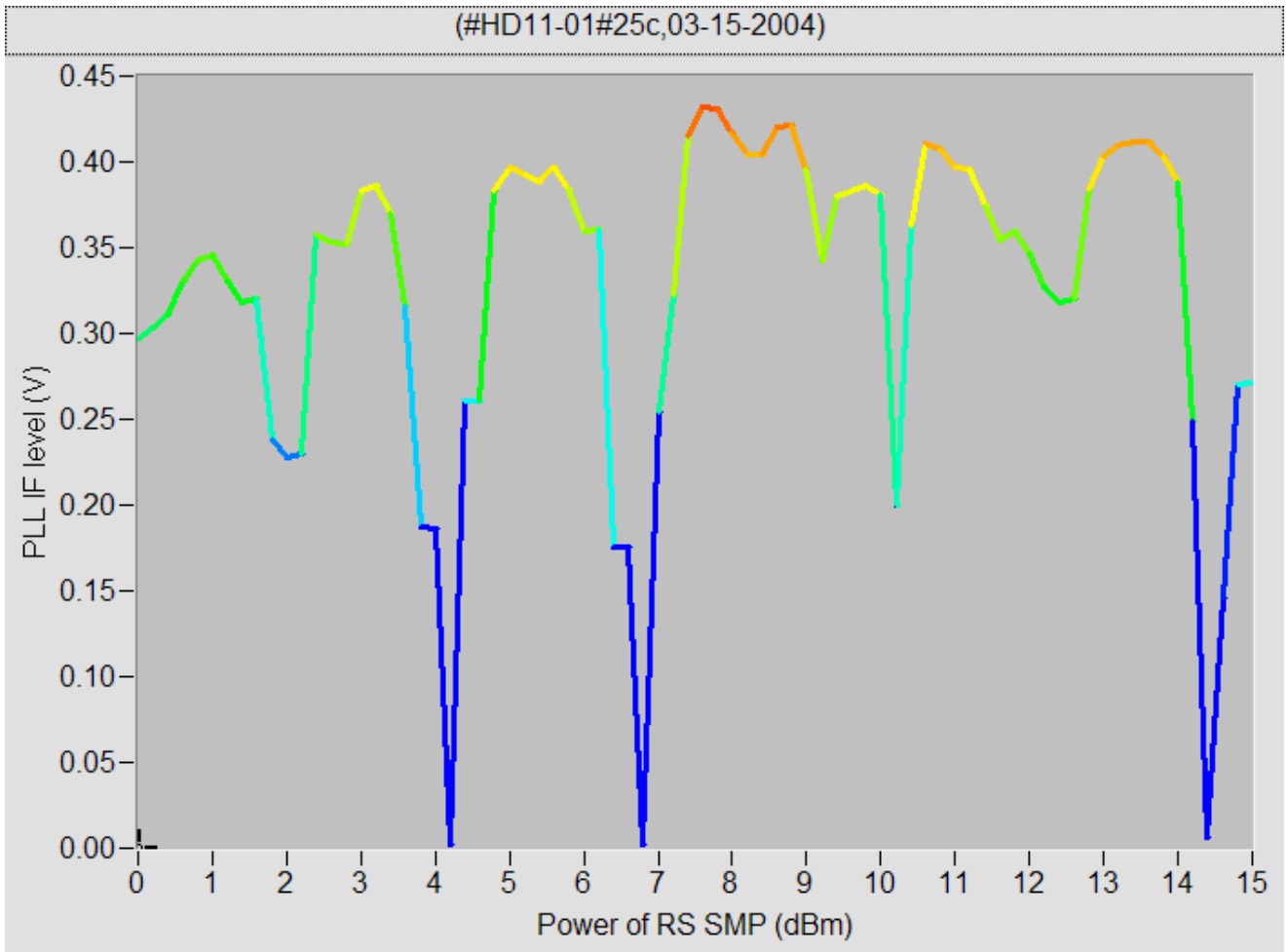




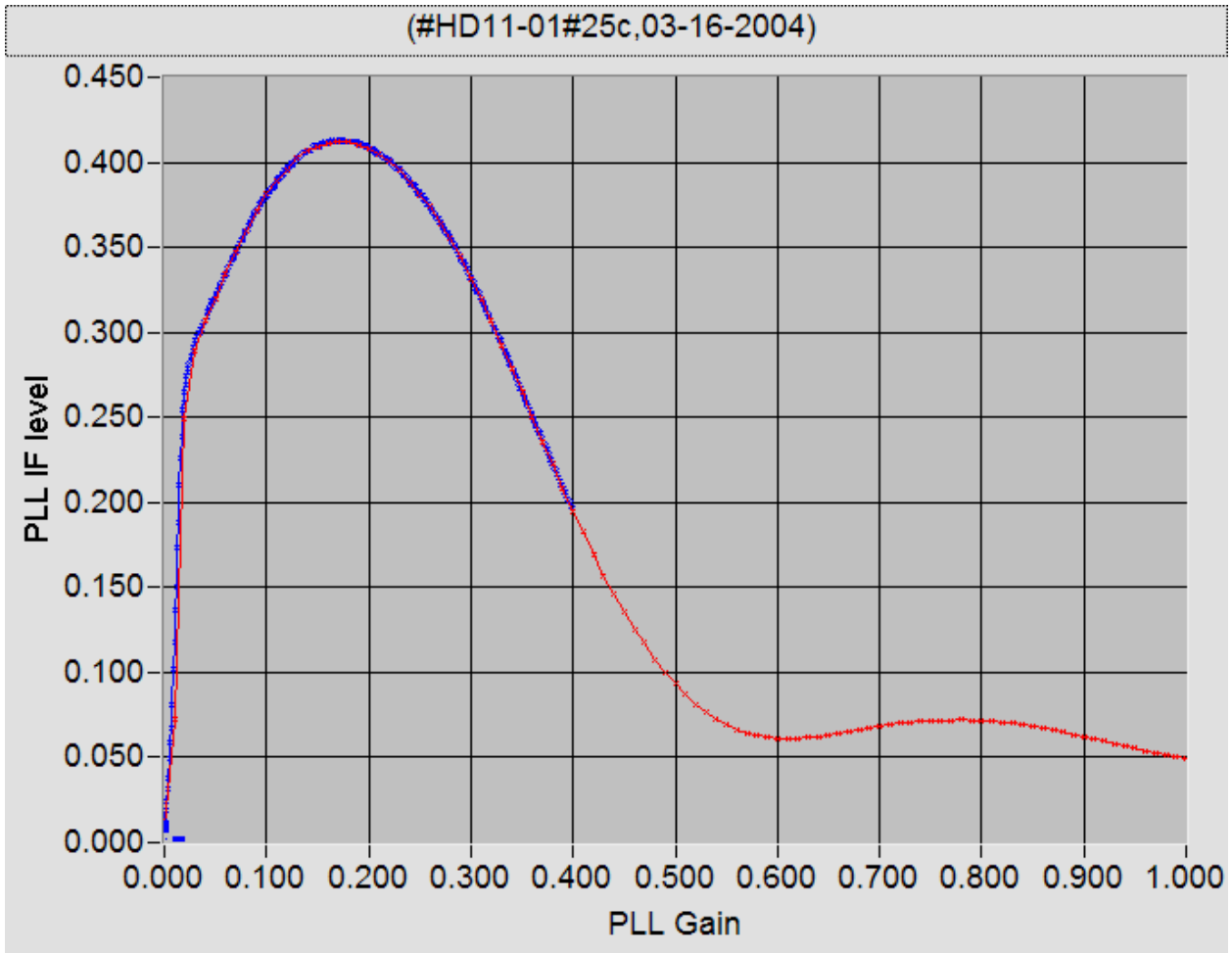
Dependence of the PLL_IF level on HM bias voltage at 2 values of synthesizer power (13.25 dBm – red and 8.5 dBm – blue)



Dependence of the PLL_IF level on synthesizer power at HM bias voltage = 0.0 mV.



Dependence of the PLL_IF level on the PLL Gain setting



Algorithms for TSCU (block diagram)

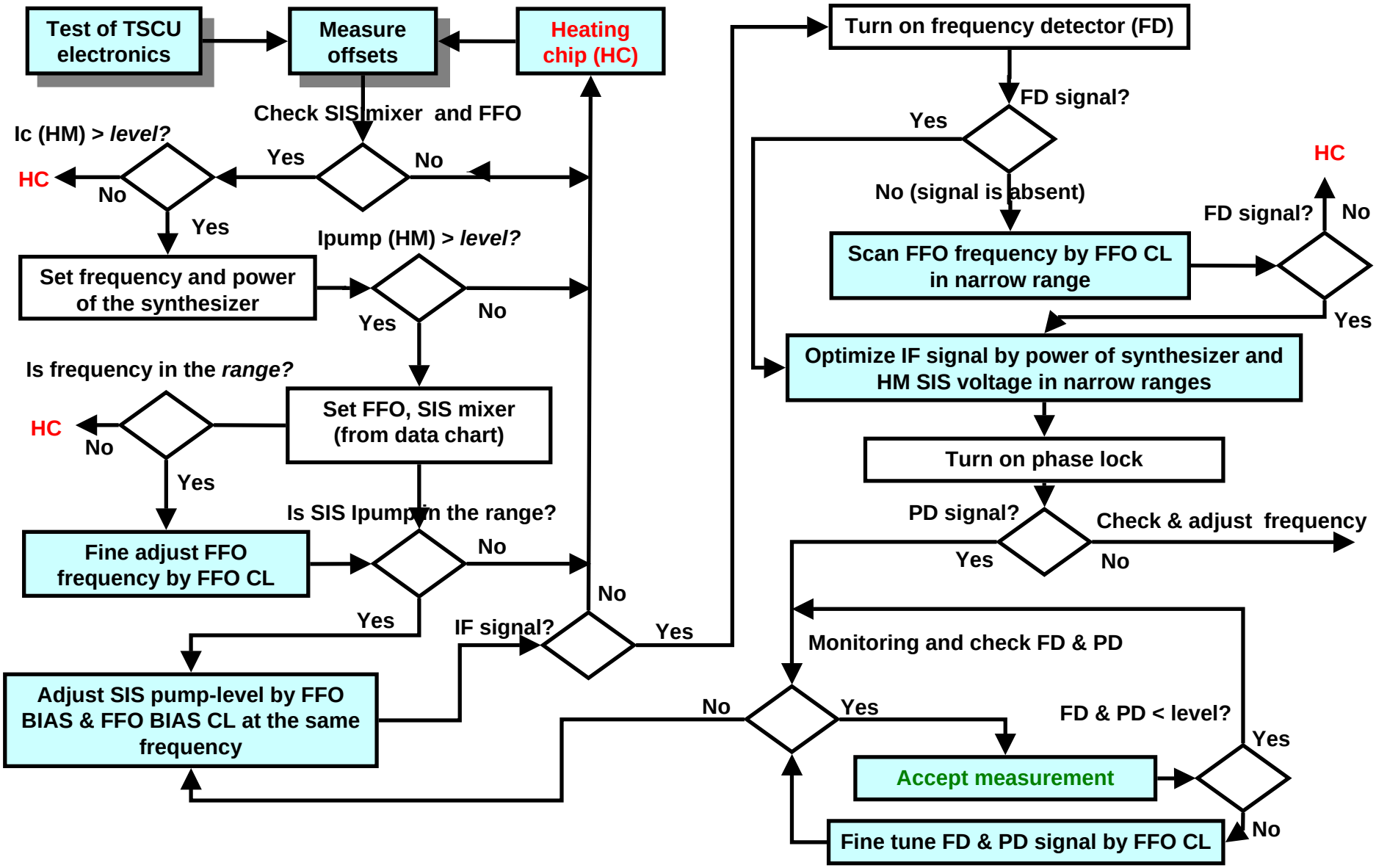
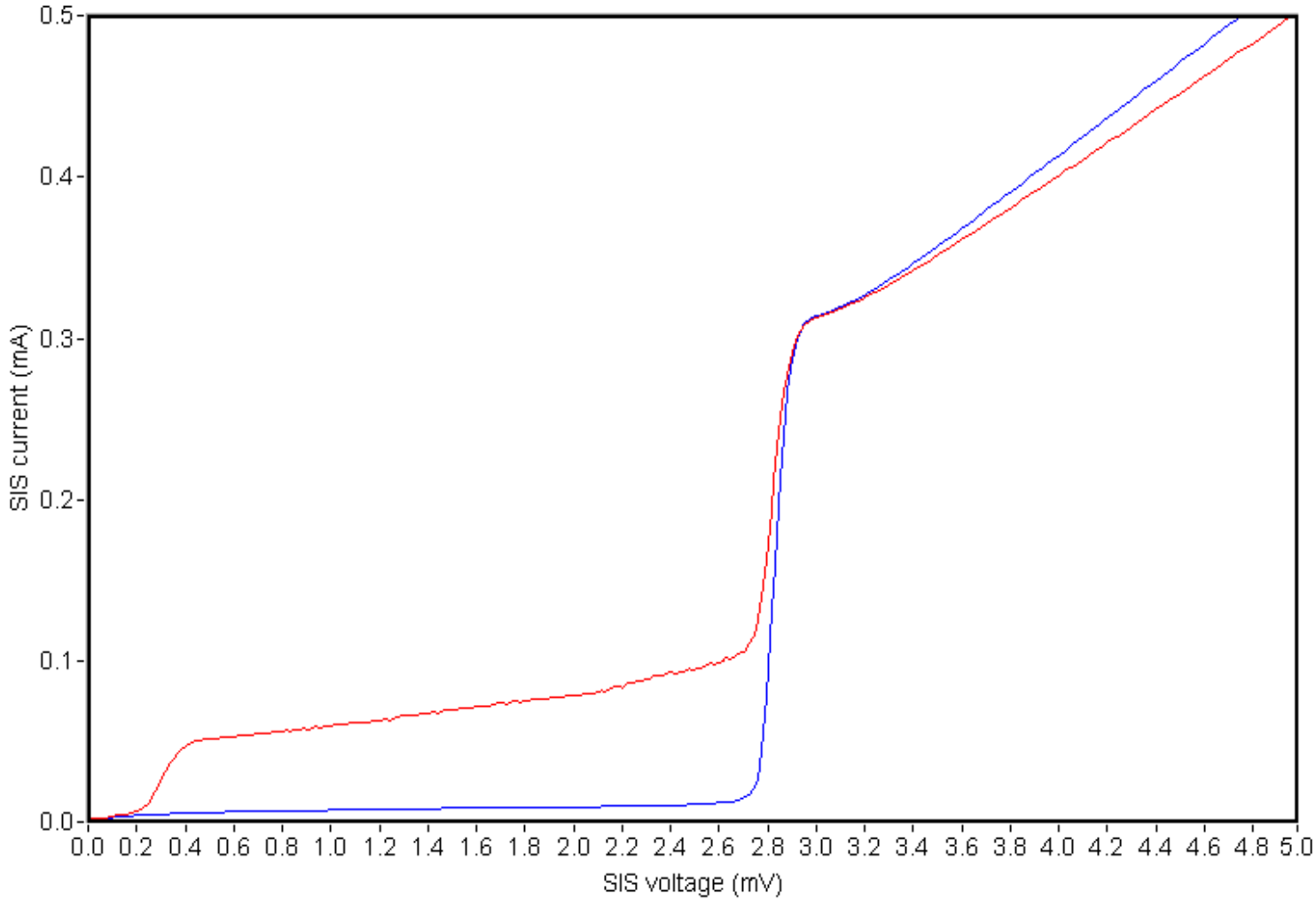


Table of available T2 SIR batches

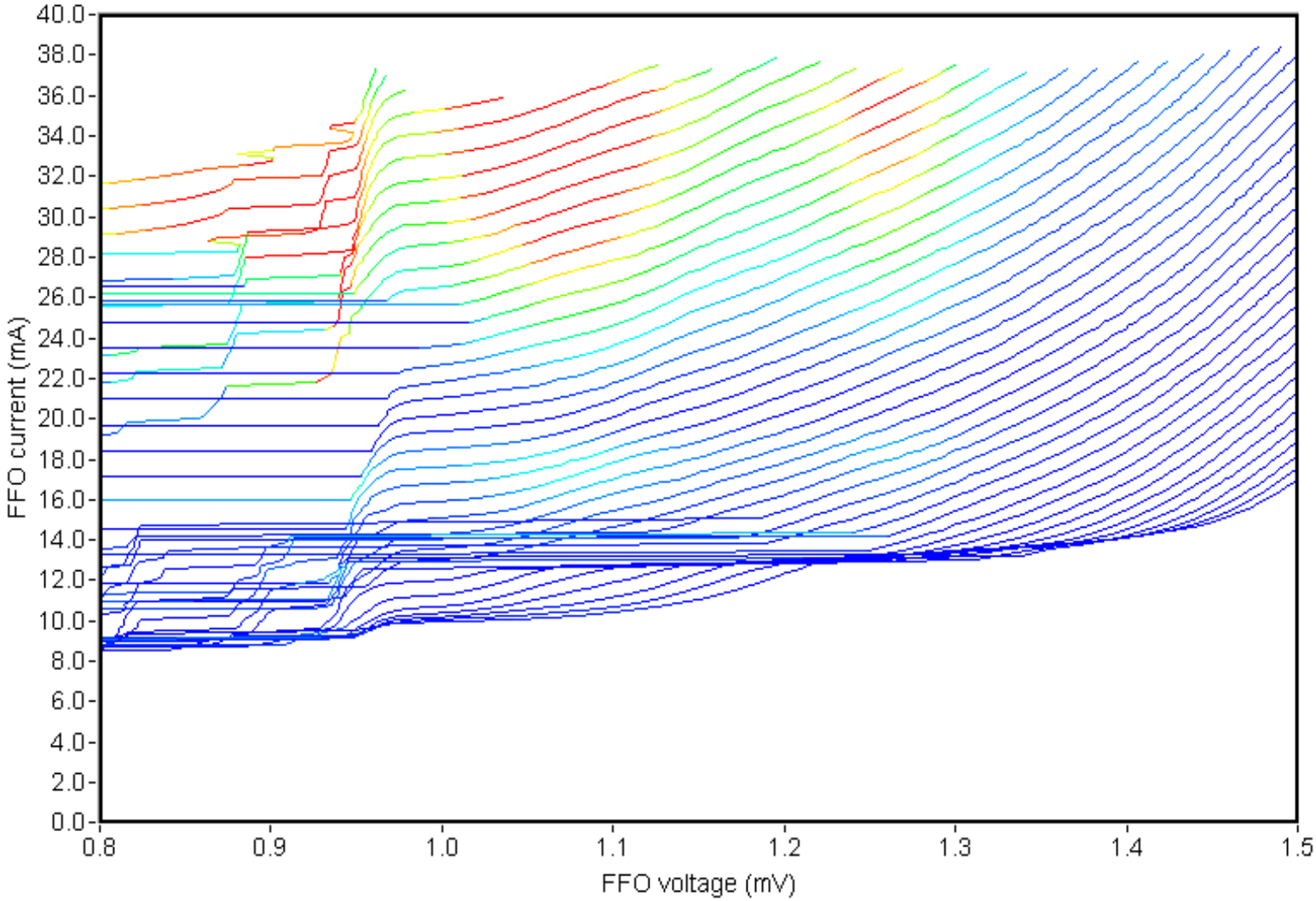
#	Date	Substrate	RnS	
			SIS	FFO
T2011 T2012	20/10/2003-25/10/2003	Si 300 μm, one side polished	28-30	
T2021 T2022	27/10/2003-6/11/2003	Si 300 μm, one side polished	28-30	
T2031 T2032	31/10/2003-12/11/2003	Si 300 μm one side polished	28-30	
T2041	13/10/2003-20/10/2003	Si 520 μm, two side polished	28-30	
T2051 T2052	13/10/2003-20/10/2003	Si 520 μm, two side polished	20	38
T2061 T2062	20/01/2004-30/01/2004	Si 520 μm, two side polished	20-24	
T2071 T2072	20/01/2004-30/01/2004	Si 520 μm, two side polished	15-17	37-40
T2081 T2082	9/02/2004-20/02/2004	Si 520 μm, two side polished	15-17	37-40

Dipstick Tests: Twin-SIS Mixer Pump Level

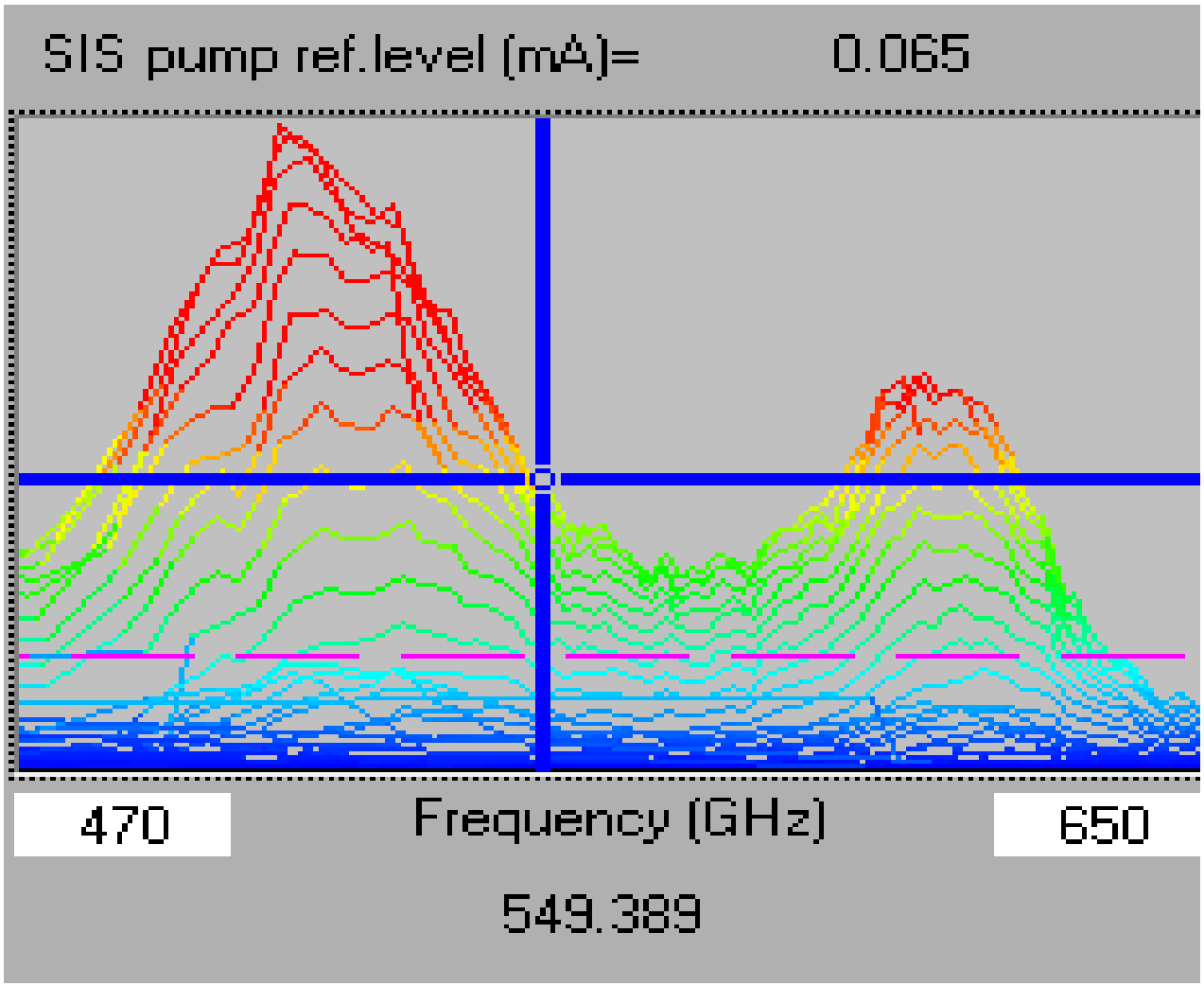
f = 613 GHz



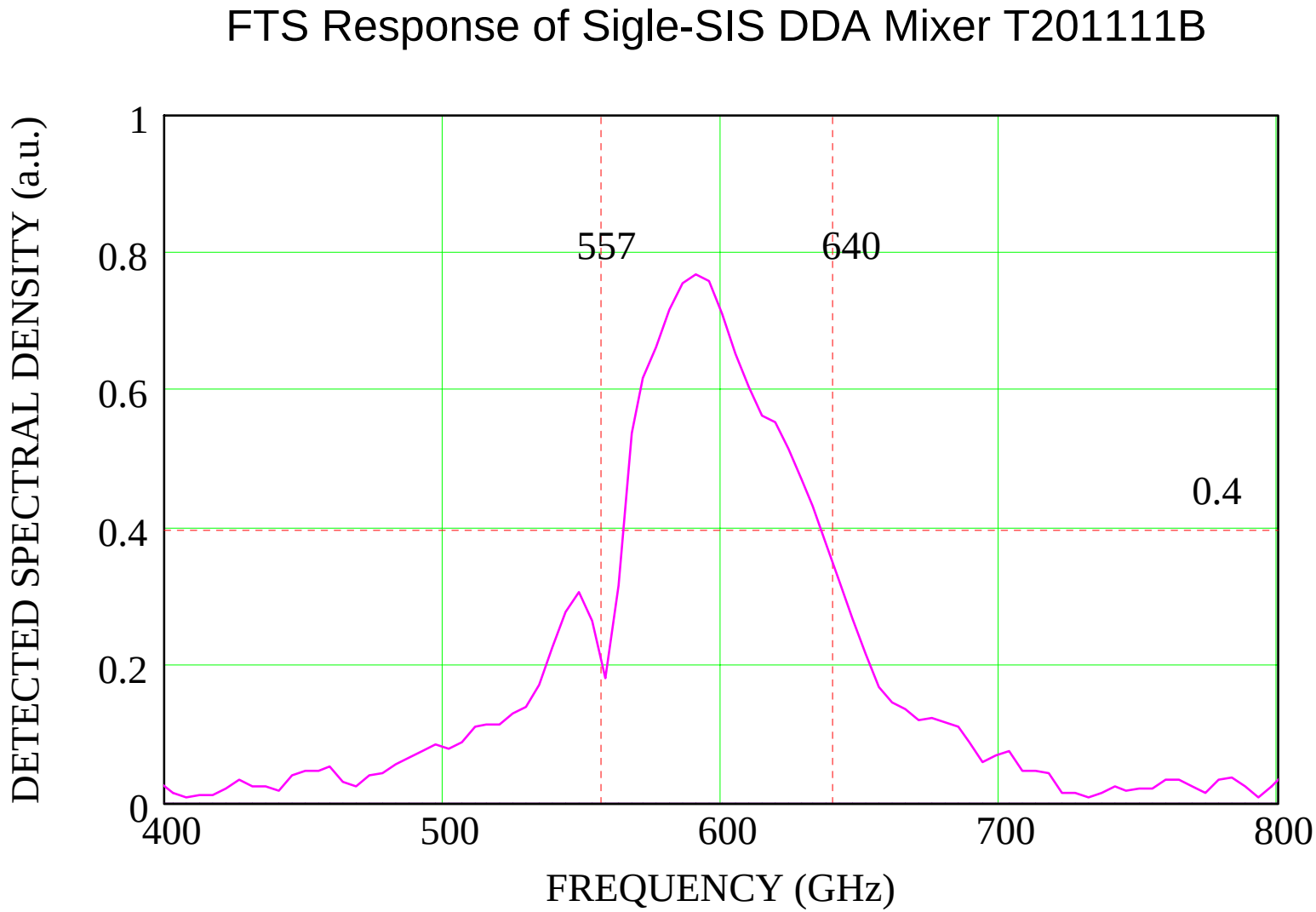
Dipstick Test: FFO Power Range



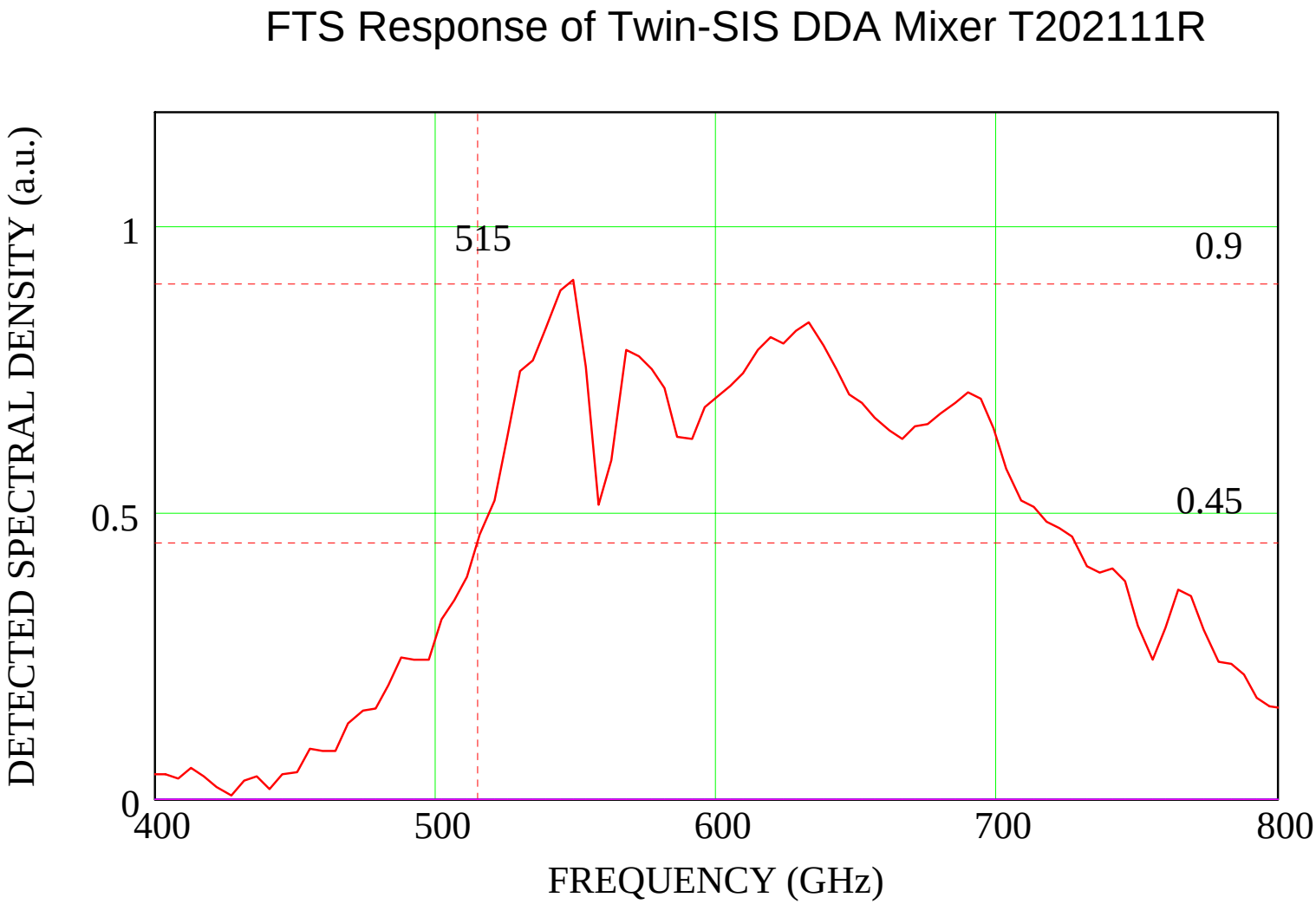
Dipstick Test: FFO Power Range



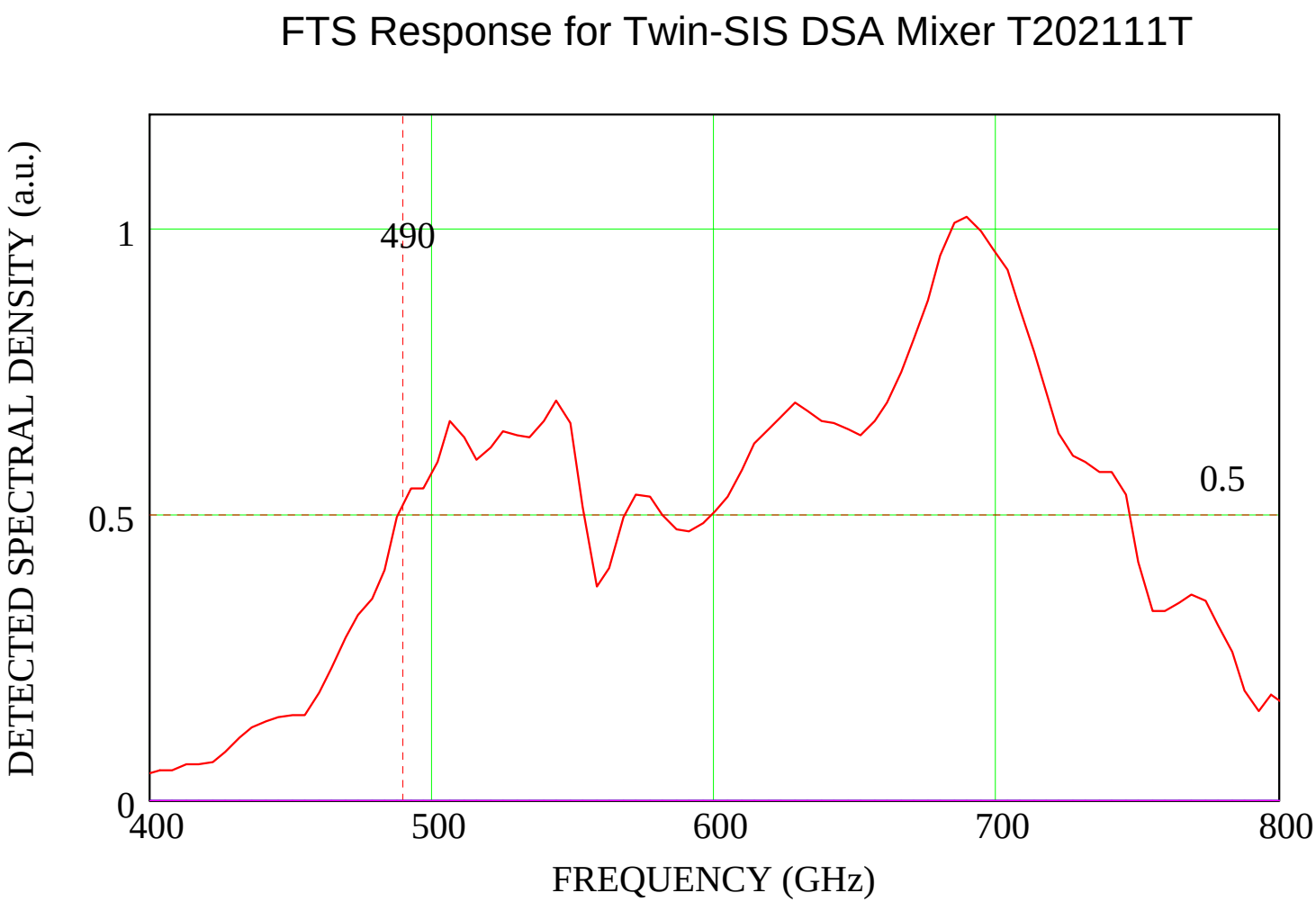
FTS Test: DDA Single-SIS Mixer



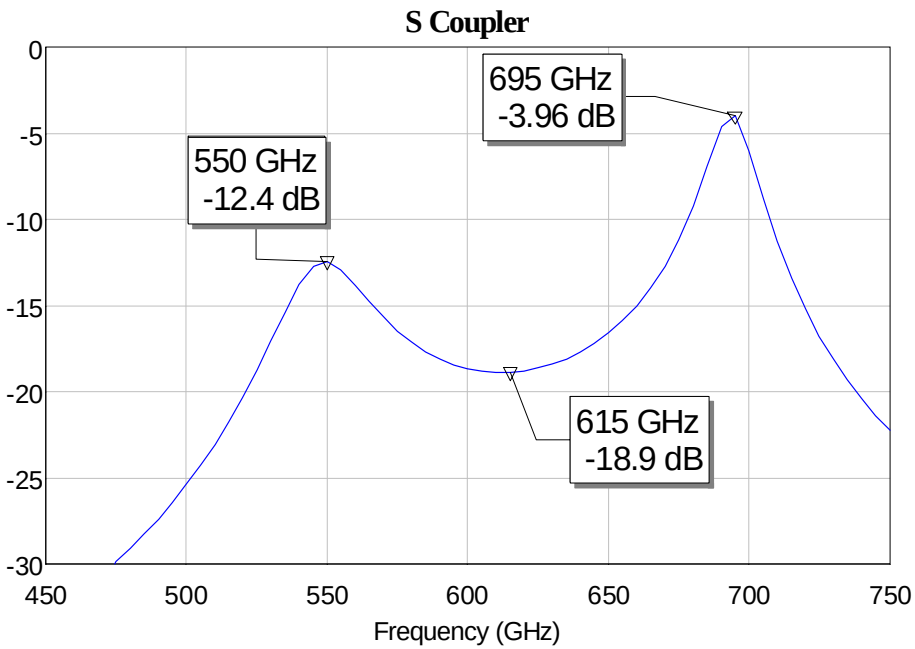
FTS Test: DDA Twin-SIS Mixer

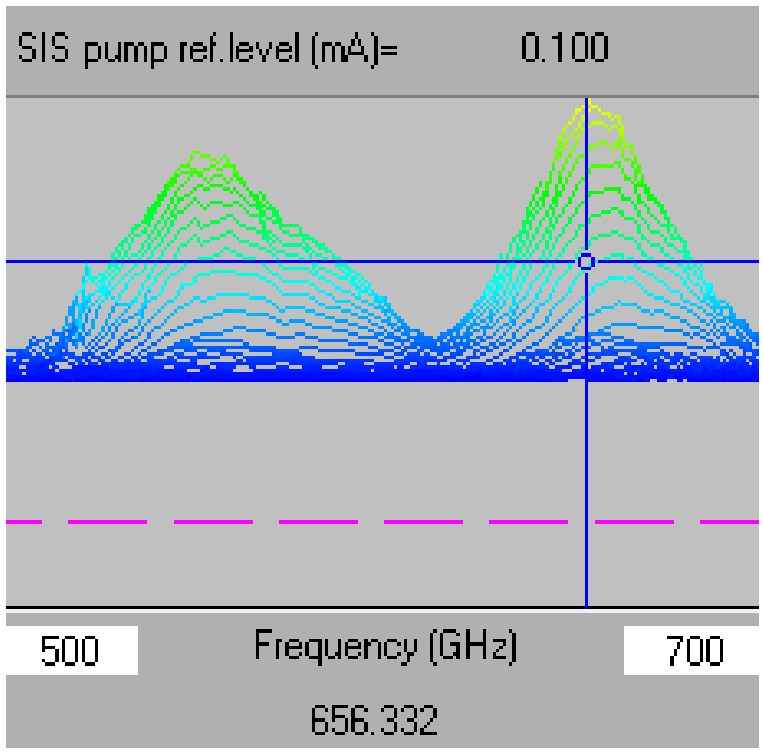


FTS Test: DSA Twin-SIS Mixer



Simulation vs. Test: Pump of Harmonic Mixer





T_{RX} Test: brief arrangement of new cryostat

Preliminary Noise Breakdown

- Y-factor 1-1.3 dB @ 600-630 GHz
- 50 μm beam splitter (BS) transparent 65% @600 GHz; T_{cold} rises from 80 K to 156 K
- TRX corrected for BS is 250-380 K
- Dewar window & two infrared filters T = 50%
- IF coupling -2.5 dB @ IF=1.5 GHz
- Final estimate 100-120 K (DSB)
- NOTE: Cooling might be insufficient

Test Summary

- ***Production of circuits is going satisfactory***
  - ✓Reproducible small area (0.8 μm^2) SIS junctions
- ***Twin SIS covers band 520-680 GHz***
  - ✓Flat response has been achieved
- ***Single-SIS as a narrow-band option***
  - ✓Single-SIS is OK for band 600-650 GHz
- ***Noise Temperature Preliminary Estimate***
  - ✓Known corrections give 120K (DSB) at IF=1.5 GHz

T2 chips selected for further receiver test

Summary of chips selected for receiver test

Sample ID	Type (design code)	Expected full performance band (GHz)	FTS band (GHz)	SIS Mixer(s)				FFO	
				R_N SIS / HM (Ω)	Q Rj/Rn a.u.	I_{CL} zeroing (mA)	Pump range f_1-f_2 of SIS / HM (GHz)	I_{step} max (mA)	$I_{CL\ FFO}$ range (mA)
T201208	F2-D2-HMT-4	500-650	500-550,600-670	17.3/6.38	27/25	50-74-101	480-650/500-700	21	11-20
T204102	F1-S2-HM-4	570-650	480-520,570-800	22.4/11.8	26/23	89	550-700/550-650	37	22-33
T201105	F1-D2-HM-4	600-625	600-700	9.56/4.11	14/23	19-55-80	480-630/620-670	32	25-29
T201103	F2-D2-HM-4	500-550 580-630	470-700	8.81/5.41	26/7	34-68-88	470-630/520-700	39	15-23
T201108	F2-D2-HM-4	500-560 600-640	600-730	10.83/6.08	25/17	36-75	480-640/520-710	32	14-26
T201215	F2-S2-HMT-4	470-560	460-550	10.88/6.54	22/26	43-80-99	440-640/530-700	18	17-24
T201219	F2-S2-HM-4	480-560	450-550	10.52/5.8	35/37	36-66-112	480-557/540-690	25	17-24

Conclusion

- **3 concepts of PL SIR for TELIS have been proposed; 2 of them experimentally proven.**
- **SIR for TELIS has been developed, fabricated and preliminary tested.**
- **All main TELIS parameters are satisfied.**
- **A number of T2 chips with suitable parameters are selected for further RF measurements.**
- **Design and parameters of FFO and HM were optimized for TELIS.**
- **Possibility to operate a PL SIR remotely has been demonstrated.**